REGISTER REFERENCE

FLIR Machine Vision Cameras

Version 4.0

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FCC Compliance

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesirable operation.

Korean EMC Certification

The KCC symbol indicates that this product complies with Korea's Electrical Communication Basic Law regarding EMC testing for electromagnetic interference (EMI) and susceptibility (EMS).

Hardware Warranty

The warranty for your camera is in the camera's Technical Reference. For detailed information on how to repair or replace your camera, please see the terms and conditions on our website.

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To view the licenses of open source packages used in this product please see What open source packages does firmware use?

Table of Contents

About This Manual

The FLIR Machine Vision Camera Register Reference documents the registers used to control all FLIR machine vision imaging products and select stereo vision products.

Not all registers are used by all cameras. This document should be used in conjunction with the camera-specific *Technical Reference* or *Getting Started Manual* to determine the full functionality offered by each camera system.

Our camera systems are complex and dynamic – if any errors or omissions are found during experimentation, please contact us using our support web form. This document is subject to change without notice.

Where to Find Information

Chapter	What You Will Find
1. Using Registers	General Register Information (page 1) Calculating Register Addresses (page 5) Absolute Value Registers (page 5)
2. Inquiry Registers	Basic Functions (page 9) Feature Presence (page 9) Feature Elements (page 11) Video Format (page 13) Video Mode (page 13) Video Frame Rate (page 15)
3. General Camera Operation	Memory Channels (page 19) Device Information (page 21) Camera Memory (page 23) Firmware Information (page 26)
4. Input/Output Control	GPIO Modes (page 29) and Pins (page 30) Strobe Registers (page 32) SIO Registers (page 35) Debouncer (page 39)
5. Video Formats, Modes, and Frame Rates	Video Format and Mode CSRs (page 41) Inquiry Registers for Format 7 (page 43)
6. Image Acquisition and Transmission	General acquisition registers (page 50) Trigger Modes (page 53)

Chapter	What You Will Find
7. Image Parameters and Control	Imaging Parameters (including Brightness, Sharpness, Hue, Saturation, Gamma, Gain, Iris) (page 62) Lookup Table (page 64) White Balance (page 67) Bayer Color Processing (page 68) Image Flip/Mirror (page 69) Shutter (page 69) Auto Exposure (page 70) High Dynamic Range (page 72) Noise Reduction (page 73) Zoom/Stretch (page 74) Embedded Image Information (page 78)
8. Troubleshooting	Support (page 81) Camera Diagnostics (page 81)
Appendix	Isochronous Packet Format (FireWire only) (page 85)
Appendix	Dragonfly only Registers (page 88)
Contacting FLIR	How to reach us. (page 92)

Document Conventions

This manual uses the following to provide you with additional information:

Note: A note that contains information that is distinct from the main body of text. For example, drawing attention to a difference between models; or a reminder of a limitation.

Warning! A note that contains a warning to proceed with caution and care, or to indicate that the information is meant for an advanced user. For example, indicating that an action may void the camera's warranty or cause damage to the camera or other equipment.

```
Code is presented in a grey box with Courier font.
```

If further information can be found in our Knowledge Base, a list of articles is provided.

Related Knowledge Base Articles

Title	Article
Title of the Article	Link to the article on the website

If there are further resources available, a link is provided either to an external website, or to the SDK.

Related Resources

Title	Link
Title of the resource	Link to the resource

1 Using Control and Status Registers

The user can monitor or control each feature of the camera through the control and status registers (CSRs) programmed into the camera firmware. These registers conform to the IIDC v1.32 standard (except where noted). *Format* tables for each 32-bit register are presented to describe the purpose of each bit that comprises the register. Bit 0 is always the most significant bit of the register value.

Register offsets and values are generally referred to in their hexadecimal forms, represented by either a '0x' before the number or 'h' after the number, e.g. the decimal number 255 can be represented as 0xFF or FFh.

The controllable fields of most registers are *Mode* and *Value*.

1.1 Modes

Each CSR has three bits for mode control, ON_OFF, One_Push and A_M_Mode (Auto/Manual mode). Each feature can have four states corresponding to the combination of mode control bits.

Note: Not all features implement all modes.

Table 1.1: CSR Mode Control Descriptions

One_Push	ON_OFF	A_M_Mode	State
N/A	0	N/A	**Off state**. Feature will be fixed value state and uncontrollable.
N/A	1	1	**Auto control state**. Camera controls feature by itself continuously.
0	1	0	**Manual control state**. User can control feature by writing value to the value field.
1 (Self clear)	1	0	**One-Push action**. Camera controls feature by itself only once and returns to the Manual control state with adjusted value.

1.2 Values

If the *Presence_Inq* bit of the register is one, the *value* field is valid and can be used for controlling the feature. The user can write control values to the *value* field only in the **Manual control state**. In the other states, the user can only read the *value*. The camera always has to show the real setting value at the *value* field if *Presence_Inq* is one.

1.3 Register Memory Map

The camera uses a 64-bit fixed addressing model. The upper 10 bits show the Bus ID, and the next six bits show the Node ID. The next 20 bits must be 1 (FFFF Fh).

Address	Register Name	Description
FFFF F000 0000h	Base address	
FFFF F000 0400h	Config ROM	
FFFF F0F0 0000h	Base address for all camera control command registers	
The following register addresses are offset from the base address, FFFF F0F0 0000h.		
000h	INITIALIZE	Camera initialize register
100h 180h	V_FORMAT_INQ V_MODE_INQ_X	Inquiry register for video format Inquiry register for video mode
200h	V_RATE_INQ_y_X	Inquiry register for video frame rate
300h	Reserved	
400h	BASIC_FUNC_INQ FEATURE_HI_INQ FEATURE_LO_INQ	Inquiry register for feature presence
500h	*Feature_Name*_INQ	Inquiry register for feature elements
600h 640h	CAM_STA_CTRL	Status and control register for camera Feature control error status register
700h	ABS_CSR_HI_INQ_x	Inquiry register for Absolute value CSR offset address
800h	Feature_Name	Status and control register for feature

The FlyCapture® API library has function calls to get and set camera register values. These function calls automatically take into account the base address. For example, to get the 32-bit value of the SHUTTER register at 0xFFFF F0F0 081C:

FlyCapture v1.x:

```
flycaptureGetCameraRegister(context, 0x81C, &ulValue);
flycaptureSetCameraRegister(context, 0x81C, ulValue);
```

FlyCapture v2.x (assuming a `camera` object named `cam`):

```
cam.ReadRegister(0x81C, &regVal);
cam.WriteRegister(0x81C, regVal, broadcast=false);
```

Broadcast is only available for FlyCapture2 and FireWire cameras. FireWire has the ability to write to multiple cameras at the same time.

1.4 Config ROM

1.4.1 Root Directory

	Offset	Bit	Description
Bus Info Block	400h	[0-7]	04h
		[8-15]	crc_length
		[16-31]	rom_crc_value
	404h	[0-7]	31h
		[8-15]	33h
		[16-23]	39h
		[24-31]	34h
	408h	[0-3]	0010 (binary)
		[4-7]	Reserved
		[8-15]	FFh
		[16-19]	max_rec
		[20]	Reserved
		[21-23]	mxrom
		[24-31]	chip_id_hi
	40Ch	[0-23]	node_vendor_id
		[24-31]	chip_id_hi
	410h	[0-31]	chip_id_lo
Root Directory	414h	[0-15]	0004h
		[16-31]	CRC
	418h	[0-7]	03h
		[8-31]	module_vendor_id
	41Ch	[0-7]	0Ch
		[8-15]	Reserved
		[16-31]	1000001111000000 (binary)
	420h	[0-7]	8Dh
		[8-31]	indirect_offset
	424h	[0-7]	D1h
		[8-31]	unit_directory_offset

1.4.2 Unit Directory

Offset	Bit	Description
0000h	[0-15]	0003h
	[16-31]	CRC

Offset	Bit	Description
0004h	[0-7]	12h
	[8-31]	unit_spec_ID (=0x00A02D)
0008h	[0-7]	13h
	[8-31]	unit_sw_version (=0x000102)
000Ch	[0-7]	D4h
	[8-31]	unit dependent directory offset

1.4.3 Unit Dependent Info

Offset	Bit	Description
0000h	[0-15]	unit_dep_info_length
	[16-31]	CRC
0004h	[0-7]	40h
	[8-31]	command_regs_base 32-bit offset from the base address of initial register space of the base address of the command registers
0008h	[0-7]	81h
	[8-31]	vendor_name_leaf The number of 32-bits from the address of the vendor_name_leaf entry to the address of the vendor_name leaf containing an ASCII representation of the vendor name of this node
000Ch	[0-7]	82h
	[8-31]	model_name_leaf The number of 32-bits from the address of the model_name_leaf entry to the address of the model_name leaf containing an ASCII representation of the model name of this node
0010h	[0-7]	38h
	[8-31]	unit_sub_sw_version the sub version information of this unit unit_sub_sw_version = 0x000000h or unspecified for IIDC v1.30 unit_sub_sw_version = 0x000010h for IIDC v1.31 unit_sub_sw_version = 0x000020h for IIDC v1.32
0014h	[0-7]	39h
	[8-31]	Reserved
0018h	[0-7]	3Ah
	[8-31]	Reserved
001Ch	[0-7]	3Bh
	[8-31]	Reserved
0020h	[0-7]	3Ch
	[8-31]	vendor_unique_info_0
0024h	[0-7]	3Dh
	[8-31]	vendor_unique_info_1
0028h	[0-7]	3Eh
	[8-31]	vendor_unique_info_2

Offset	Bit	Description
002Ch	[0-7]	3Fh
	[8-31]	vendor_unique_info_3

1.5 Calculating Base Register Addresses using 32-bit Offsets

The addresses for many CSRs, such as those that provide control over absolute values, custom video modes, PIO, SIO and strobe output, can vary between cameras. In order to provide a common mechanism across camera models for determining the location of these CSRs relative to the base address, there are fixed locations for inquiry registers that contain offsets, or pointers, to the actual offsets.

Note: To calculate the base address for an offset CSR:

1. Query the offset inquiry register.
2. Multiple the value by 4. (The value is a 32-bit offset.)
3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

For example, the Absolute Value CSRs provide minimum, maximum and current real-world values for camera properties such as gain, shutter, etc., as described in *Absolute Value Registers* (below). To determine the location of the shutter absolute value registers (code snippets use function calls included in the FlyCapture SDK, and assume a `Camera` object `cam`):

1. Read the ABS_CSR_HI_INQ_7 register 71Ch to obtain the 32-bit offset for the absolute value CSR for shutter.

```
unsigned int ulValue;
cam.ReadRegister(0x71C, &ulValue);
```

2. The ulValue is a 32-bit offset, so multiply by 4 to get the actual offset.

```
ulValue = ulValue * 4; // ulValue == 0x3C0244, actual offset == 0xF00910
```

3. The actual offset 0xF00910 represents the offset from the base address 0xFFFF Fxxx xxxx. Since the PGR FlyCapture API automatically takes into account the base offset 0xFFFF F0F0 0000, the actual offset in this example would be 0x910.

```
ulValue = ulValue & 0xFFFF;
```

1.6 Absolute Value Registers

Many FLIR machine vision cameras implement “absolute” modes for various camera settings that report real-world values, such as shutter time in seconds (s) and gain value in decibels (dB). Using these absolute values is easier and more efficient than applying complex conversion formulas to the information in the *Value* field of the

associated Control and Status Register. A relative value does not always translate to the same absolute value. Two properties that can affect this relationship are pixel clock frequency and horizontal line frequency. These properties are, in turn, affected by such properties as resolution, frame rate, region of interest (ROI) size and position, and packet size. Additionally, conversion formulas can change between firmware versions. We therefore recommend using absolute value registers, where possible, to determine camera values.

1.6.1 Setting Absolute Value Register Values

For absolute values to be used, the associated feature CSR must be set to use absolute values.

Field	Bit	Description
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.

In the FlyCapture API, this can also be done by setting the `absControl` member of the of the desired property structure to true.

1.6.2 Absolute Value Offset Addresses

The following set of registers indicates the locations of the absolute value registers. Not all cameras use all registers.

Note: To calculate the base address for an offset CSR:

1. Query the offset inquiry register.
2. Multiple the value by 4. (The value is a 32-bit offset.)
3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

32-bit Offsets for Absolute Value Registers

Offset	Name	Bit	Description
700h	ABS_CSR_HI_INQ_0	[0..31]	Brightness
704h	ABS_CSR_HI_INQ_1	[0..31]	Auto Exposure
708h	ABS_CSR_HI_INQ_2	[0..31]	Sharpness
710h	ABS_CSR_HI_INQ_4	[0..31]	Hue
714h	ABS_CSR_HI_INQ_5	[0..31]	Saturation
718h	ABS_CSR_HI_INQ_6	[0..31]	Gamma
71Ch	ABS_CSR_HI_INQ_7	[0..31]	Shutter
720h	ABS_CSR_HI_INQ_8	[0..31]	Gain
724h	ABS_CSR_HI_INQ_9	[0..31]	Iris
734h	ABS_CSR_HI_INQ_13	[0..31]	Trigger Delay
73Ch	ABS_CSR_HI_INQ_15	[0..31]	Frame Rate
7C4h	ABS_CSR_LO_INQ_1	[0..31]	Pan
7C8h	ABS_CSR_LO_INQ_2	[0..31]	Tilt

Each set of absolute value CSRs consists of three registers as follows:

Offset	Name	Field	Bit	Description
Base + 000h	Absolute Value	Min_Value	[0-31]	Minimum value for this feature. Read only.
Base + 004h		Max_Value	[0-31]	Maximum value for this feature. Read only.
Base + 008h		Value	[0-31]	Current value of this feature.

For example:

Offset	Name	Field	Bit	Description
704h	ABS_CSR_HI_INQ_1		[0..31]	Auto Exposure.
Base + 0h	ABS_VAL_AUTO_EXPOSURE	Min_Value	[0-31]	Min auto exposure value.
Base + 4h		Max_Value	[0-31]	Max auto exposure value.
Base + 8h		Value	[0-31]	Current auto exposure value.

1.6.3 Units of Value for Absolute Value CSR Registers

The following tables describe the real-world units that are used for the absolute value registers. Each value is either Absolute (value is an absolute value) or Relative (value is an absolute value, but the reference is system dependent).

Feature	Function	Unit	Unit Description	Reference point	Value Type
Brightness	Black level offset	%		—	Absolute
Auto Exposure	Auto Exposure	EV	exposure value	0	Relative
Sharpness	Sharpness				
Hue	Hue	deg	degree	0	Relative
Saturation	Saturation	%		100	Relative
Gamma					
Shutter	Integration time	s	seconds	—	Absolute
Gain	Circuit gain	dB	decibel	0	Relative
Iris	Iris	F	F number	—	Absolute
Trigger_Delay	Trigger Delay	S	seconds	—	Absolute
Frame_Rate	Frame rate	fps	frames per second	—	Absolute
Pan	Pan				
Tilt	Tilt				

1.6.4 Determining Absolute Value Register Values

The Absolute Value CSRs store 32-bit floating-point values with IEEE/REAL*4 format. To programmatically determine the floating point equivalents of the minimum, maximum and current hexadecimal values for a property such as shutter, using the FlyCapture SDK:

1. Read the ABS_CSR_HI_INQ_7 register 71Ch to obtain the 32-bit offset for the absolute value CSR for shutter.

```
cam.ReadRegister(context, 0x71C, &ulValue);
```

2. The ulValue is a 32-bit offset, so multiply by 4 to get the actual offset.

```
ulValue = ulValue * 4; // ulValue == 0x3C0244, actual offset == 0xF00910
```

This offset represents the offset from the base address 0xFFFF Fxxx xxxx. Since the PGR FlyCapture API automatically takes into account the base offset 0xFFFF F0F0 0000, the actual offset in this example would be 0x910.

3. Use the offset obtained to read the min, max and current absolute values and convert the 32-bit hexadecimal values to floating point.

```
// declare a union of a floating point and unsigned long
typedef union _AbsValueConversion
{
 unsigned long ulValue;
 float fValue;
} AbsValueConversion;
 typedef union _AbsValueConversion
 {
 unsigned long ulValue;
 float fValue;
 } AbsValueConversion;
 float fMinShutter, fMaxShutter, fCurShutter;AbsValueConversion minShutter,
maxShutter, curShutter;
 // read the 32-bit hex value into the unsigned long member
 cam.ReadRegister(context, 0x910, &minShutter.ulValue );
 cam.ReadRegister(context, 0x914, &maxShutter.ulValue );
 cam.ReadRegister(context, 0x918, &curShutter.ulValue );
 fMinShutter = minShutter.fValue;
 fMaxShutter = maxShutter.fValue;
 fCurShutter = curShutter.fValue;
```

Note: To get and set absolute values using the FlyCapture SDK, use the `GetProperty` and `SetProperty` functions to get or set the `absValue` member of the `Property` struct. Refer to the FlyCapture SDK Help for function definitions.

2 Inquiry Registers

2.1 Basic Functions Inquiry Registers

The following registers show which basic functions are implemented on the camera.

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
400h	BASIC_ FUNC_ INQ	Advanced_Feature_Inq	[0]	Inquiry for advanced feature. (Vendor Unique Features)
		Vmode_Error_Status_Inq	[1]	Inquiry for existence of Vmode_Error_Status register
		Feature_Control_Error_Status_ Inq	[2]	Inquiry for existence of Feature_Control_ Error_Status register
		Opt_Func_CSR_Inq	[3]	Inquiry for optional function CSR.
			[4-7]	Reserved
		1394.b_mode_Capability	[8]	Inquiry for 1394.b mode capability
			[9-15]	Reserved
		Cam_Power_Cntl	[16]	Camera process power ON/OFF capability
			[17-18]	Reserved
		One_Shot_Inq	[19]	One shot transmission capability
		Multi_Shot_Inq	[20]	Multi shot transmission capability
		Retransmit_Inq	[21]	Retransmit latest image capability (One_ shot/Retransmit)
		Image_Buffer_Inq	[22]	Image buffer capability (Multi_shot/Image_Buffer)
			[23-27]	Reserved
		Memory_Channel	[28-31]	Maximum memory channel number (N) Memory channel 0 = Factory setting memory 1 = Memory Ch 1 2 = Memory Ch 2 : N= Memory Ch N If 0000, user memory is not available.

2.2 Feature Presence Inquiry Registers

The following registers show the presence of the camera features or optional functions implemented on the camera.

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
404h	Feature_Hi_Inq	Brightness	[0]	Brightness Control
		Auto_Exposure	[1]	Auto Exposure Control
		Sharpness	[2]	Sharpness Control
		White_Balance	[3]	White Balance Control
		Hue	[4]	Hue Control
		Saturation	[5]	Saturation Control
		Gamma	[6]	Gamma Control
		Shutter	[7]	Shutter Speed Control
		Gain	[8]	Gain Control
		Iris	[9]	IRIS Control
		Focus	[10]	Focus Control
		Temperature	[11]	Temperature Control
		Trigger	[12]	Trigger Control
		Trigger_Delay	[13	Trigger Delay Control
		White_Shading	[14]	White Shading Compensation Control
		Frame_Rate	[15]	Frame rate prioritize control
			[16-31]	Reserved
408h	Feature_Lo_Inq	Zoom	[0]	Zoom Control
		Pan	[1]	Pan Control
		Tilt	[2]	Tilt Control
		Optical Filter	[3]	Optical Filter Control
			[4-15]	Reserved
		Capture_Size	[16]	Capture image size for Format_6
		Capture_Quality	[17]	Capture image quality for Format_6
			[18-31]	Reserved
40Ch	Opt_Function_Inq	-	[0]	Reserved
		PIO	[1]	Parallel input/output control
		SIO	[2]	Serial Input/output control
		Strobe_Output	[3]	Strobe signal output
		Lookup_Table	[4]	Lookup table control
		-	[5-31]	Reserved
410h-47Fh	Reserved			
480h	Advanced_Feature_Inq	Advanced_Feature_Quadlet_Offset	[0-31]	32-bit offset of the advanced feature CSRs from the base address of initial register space. (Vendor unique)
484h	PIO_Control_CSR_Inq	PIO_Control_Quadlet_Offset	[0-31]	32-bit offset of the PIO control CSRs from the base address of initial register space.

Offset	Name	Field	Bit	Description
488h	SIO_Control_CSR_Inq	SIO_Control_ Quadlet_Offset	[0-31]	32-bit offset of the SIO control CSRs from the base address of initial register space.
48Ch	Strobe_Output_CSR_ Inq	Strobe_Output_ Quadlet_Offset	[0-31]	32-bit offset of the strobe output signal CSRs from the base address of initial register space.
490h	Lookup_Table_CSR_ Inq	Lookup_Table_ Quadlet_Offset	[0-31]	32-bit offset of the Lookup Table CSRs from the baes address of initial register space.

2.3 Feature Elements Inquiry Registers

The following registers show the presence of specific features, modes and minimum and maximum values for each of the camera features or optional functions implemented by the camera.

(Bit values = 0: Not Available, 1: Available)

Offset	Name	Field	Bit	Description
500h	BRIGHTNESS_INQ	Presence_Inq	[0]	Presence of this feature
		Abs_Control_Inq	[1]	Absolute value control
			[2]	Reserved
		One_Push_Inq	[3]	One push mode (controlled automatically only once)
		ReadOut_Inq	[4]	Ability to read the value of this feature
		On_Off_Inq	[5]	Ability to switch feature ON and OFF
		Auto_Inq	[6]	Auto mode (controlled automatically)
		Manual_Inq	[7]	Manual mode (controlled by user)
		Min_Value	[8-19]	Minimum value for this feature control
		Max_Value	[20-31]	Maximum value for this feature control
504h	AUTO_EXPOSURE_ INQ	Same format as the BRIGHTNESS_INQ register		
508h	SHARPNESS_INQ	Same format as the BRIGHTNESS_INQ register		
50Ch	WHITE_BALANCE_ INQ	Same format as the BRIGHTNESS_INQ register		
510h	HUE_INQ	Same format as the BRIGHTNESS_INQ register		
514h	SATURATION_INQ	Same format as the BRIGHTNESS_INQ register		
518h	GAMMA_INQ	Same format as the BRIGHTNESS_INQ register		
51Ch	SHUTTER_INQ	Same format as the BRIGHTNESS_INQ register		
520h	GAIN_INQ	Same format as the BRIGHTNESS_INQ register		
524h	IRIS_INQ	Same format as the BRIGHTNESS_INQ register		
528h	FOCUS_INQ	Same format as the BRIGHTNESS_INQ register		
52Ch	TEMPERATURE_INQ	Same format as the BRIGHTNESS_INQ register		

Offset	Name	Field	Bit	Description
530h	TRIGGER_INQ	Presence_Inq	[0]	Presence of this feature
		Abs_Control_Inq	[1]	Absolute value control
			[2-3]	Reserved
		ReadOut_Inq	[4]	Ability to read the value of this feature
		On_Off_Inq	[5]	Ability to switch feature ON and OFF
		Polarity_Inq	[6]	Ability to change trigger input polarity
		Value_Read_Inq	[7]	Ability to read raw trigger input
		Trigger_Source0_Inq	[8]	Presence of Trigger Source 0 ID=0
		Trigger_Source1_Inq	[9]	Presence of Trigger Source 1 ID=1
		Trigger_Source2_Inq	[10]	Presence of Trigger Source 2 ID=2
		Trigger_Source3_Inq	[11]	Presence of Trigger Source 3 ID=3
			[12-14]	Reserved
		Software_Trigger_Inq	[15]	Presence of Software Trigger ID=7
		Trigger_Mode0_Inq	[16]	Presence of Trigger Mode 0
		Trigger_Mode1_Inq	[17]	Presence of Trigger Mode 1
		Trigger_Mode2_Inq	[18]	Presence of Trigger Mode 2
		Trigger_Mode3_Inq	[19]	Presence of Trigger Mode 3
		Trigger_Mode4_Inq	[20]	Presence of Trigger Mode 4
		Trigger_Mode5_Inq	[21]	Presence of Trigger Mode 5
			[22-29]	Reserved
		Trigger_Mode14_Inq	[30]	Presence of Trigger Mode 14 (Vendor unique trigger mode 0)
		Trigger_Mode15_Inq	[31]	Presence of Trigger Mode 15 (Vendor unique trigger mode 1)
534h	TRIGGER_DLY_INQ	Presence_Inq	[0]	Presence of this feature
		Abs_Control_Inq	[1]	Absolute value control
			[2]	Reserved
		One_Push_Inq	[3]	One push mode (controlled automatically only once)
		ReadOut_Inq	[4]	Ability to read the value of this feature
		On_Off_Inq	[5]	Ability to switch feature ON and OFF
			[6-7]	Reserved
		Min_Value	[8-19]	Minimum value for this feature control
		Max_Value	[20-31]	Maximum value for this feature control

Offset	Name	Field	Bit	Description
538h	WHITE_SHD_INQ	Same format as the BRIGHTNESS_INQ register		
53Ch	FRAME_RATE_INQ	Same format as the BRIGHTNESS_INQ register		
540h : 57Ch	Reserved for other FEATURE_HI_INQ			
580h	ZOOM_INQ	Same format as the BRIGHTNESS_INQ register		
584h	PAN_INQ	Same format as the BRIGHTNESS_INQ register		
588h	TILT_INQ	Same format as the BRIGHTNESS_INQ register		
58Ch	OPTICAL_FILTER_INQ	Same format as the BRIGHTNESS_INQ register		
1220h	NOISE_REDUCTION_INQ	Presence_Inq	[0]	Presence of this feature
			[1-3]	Reserved
		ReadOut_Inq	[4]	Ability to read the value of this feature
		On_Off_Inq	[5]	Ability to switch feature ON and OFF
		Auto_Inq	[6]	Auto mode (controlled automatically)
		Manual_Inq	[7]	Manual mode (controlled by user)
			[8-31]	Reserved

2.4 Video Format Inquiry Registers

The following registers may be used to determine the video formats that are available with the camera.

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
100h	V_FORMAT_INQ	Format_0	[0]	VGA non-compressed format (160x120 through 640x480)
		Format_1	[1]	Super VGA non-compressed format (1) (800x600 through 1024x768)
		Format_2	[2]	Super VGA non-compressed format (2) (1280x960 through 1600x1200)
		Format_x	[3-5]	Reserved for other formats
		Format_6	[6]	Still Image Format
		Format_7	[7]	Partial Image Size Format
			[8-31]	Reserved

2.5 Video Mode Inquiry Registers

The following registers may be used to determine the video modes that are available with the camera.

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
180h	V_MODE_INQ_O (Format 0)	Mode_0	[0]	160 x 120 YUV(4:4:4) Mode (24 bits/pixel)
		Mode_1	[1]	320 x 240 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_2	[2]	640 x 480 YUV(4:1:1) Mode (12 bits/pixel)
		Mode_3	[3]	640 x 480 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_4	[4]	640 x 480 RGB Mode (24 bits/pixel)
		Mode_5	[5]	640 x 480 Y8 (Mono) Mode (8 bits/pixel)
		Mode_6	[6]	640 x 480 Y16 (Mono16) Mode (16 bits/pixel)
			[7-31]	Reserved
184h	V_MODE_INQ_1 (Format 1)	Mode_0	[0]	800 x 600 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_1	[1]	800 x 600 RGB Mode (24 bits/pixel)
		Mode_2	[2]	800 x 600 Y (Mono) Mode (8 bits/pixel)
		Mode_3	[3]	1024 x 768 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_4	[4]	1024 x 768 RGB Mode (24 bits/pixel)
		Mode_5	[5]	1024 x 768 Y (Mono) Mode (8 bits/pixel)
		Mode_6	[6]	800 x 600 Y (Mono16) Mode (16 bits/pixel)
		Mode_7	[7]	1024 x 768 Y (Mono16) Mode (16 bits/pixel)
			[8-31]	Reserved
188h	V_MODE_INQ_2 (Format 2)	Mode_0	[0]	1280 x 960 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_1	[1]	1280 x 960 RGB Mode (24 bits/pixel)
		Mode_2	[2]	1280 x 960 Y (Mono) Mode (8 bits/pixel)
		Mode_3	[3]	1600 x 1200 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_4	[4]	1600 x 1200 RGB Mode (24 bits/pixel)
		Mode_5	[5]	1600 x 1200 Y (Mono) Mode (8 bits/pixel)
		Mode_6	[6]	1280 x 960 Y (Mono16) Mode (16 bits/pixel)
		Mode_7	[7]	1600 x 1200 Y (Mono16) Mode (16 bits/pixel)
			[8-31]	Reserved
18Ch : 197h	Reserved			
19Ch	V_MODE_INQ_7 (Format 7)	Mode_0	[0]	Format 7 Mode 0
		Mode_1	[1]	Format 7 Mode 1
		Mode_2	[2]	Format 7 Mode 2
		Mode_3	[3]	Format 7 Mode 3
		Mode_4	[4]	Format 7 Mode 4
		Mode_5	[5]	Format 7 Mode 5
		Mode_6	[6]	Format 7 Mode 6
		Mode_7	[7]	Format 7 Mode 7
			[8-31]	Reserved

2.6 Video Frame Rate Inquiry Registers

This set of registers allows the user to query the available frame rates for all Formats and Modes.

(Bit values = 0: Not Available, 1: Available)

Offset	Name	Field	Bit	Description
200h	V_RATE_INQ_0_0 (Format 0, Mode 0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps
		FrameRate_7	[7]	240 fps
			[8-31]	Reserved
204h	V_RATE_INQ_0_1 (Format 0, Mode 1)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps
		FrameRate_7	[7]	240 fps
			[8-31]	Reserved
208h	V_RATE_INQ_0_2 (Format 0, Mode 2)	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		
20Ch	V_RATE_INQ_0_3 (Format 0, Mode 3)	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		
210h	V_RATE_INQ_0_4 (Format 0, Mode 4)	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		
214h	V_RATE_INQ_0_5 (Format 0, Mode 5)	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		
218h	V_RATE_INQ_0_6 (Format 0, Mode 6)	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		
21Ch : 21Fh	Reserved			

Offset	Name	Field	Bit	Description
220h	V_RATE_INQ_1_0 (Format 1, Mode 0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps
		FrameRate_7	[7]	240 fps
			[8-31]	Reserved
224h	V_RATE_INQ_1_1 (Format 1, Mode 1)	Same format as V_RATE_INQ_0_0 Register (Format 0, Mode 0)		
228h	V_RATE_INQ_1_2 (Format 1, Mode 2)	Same format as V_RATE_INQ_0_0 Register (Format 0, Mode 0)		
22Ch	V_RATE_INQ_1_3 (Format 1, Mode 3)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
230h	V_RATE_INQ_1_4 (Format 1, Mode 4)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
234h	V_RATE_INQ_1_5 (Format 1, Mode 5)	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		
238h	V_RATE_INQ_1_6 (Format 1, Mode 6)	Same format as V_RATE_INQ_1_0 register (Format 1, Mode 0)		
23Ch	V_RATE_INQ_1_7 (Format 1, Mode 7)	Same format as V_RATE_INQ_1_3 register (Format 1, Mode 3)		
240h	V_RATE_INQ_2_0 (Format 2, Mode 0)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)		
244h	V_RATE_INQ_2_1 (Format 2, Mode 1)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)		

Offset	Name	Field	Bit	Description
248h	V_RATE_INQ_2_2 (Format 2, Mode 2)	Same format as V_RATE_INQ_1_3 register (Format 1, Mode 3)		
24Ch	V_RATE_INQ_2_3 (Format 2, Mode 3)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)		
250h	V_RATE_INQ_2_4 (Format 2, Mode 4)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	Reserved
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
254h	V_RATE_INQ_2_5 (Format 2, Mode 5)	Same format as V_RATE_INQ_1_3 register (Format 1, Mode 3)		
258h	V_RATE_INQ_2_6 (Format 2, Mode 6)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)		
25Ch	V_RATE_INQ_2_7 (Format 2, Mode 7)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)		
260h : 2BFh	Reserved			
2E0h	V_CSR_INQ_7_0	Mode_0	[0-31]	CSR 32-bit offset for Format 7 Mode 0
2E4h	V_CSR_INQ_7_1	Mode_1	[0-31]	CSR 32-bit offset for Format 7 Mode 1
2E8h	V_CSR_INQ_7_2	Mode_2	[0-31]	CSR 32-bit offset for Format 7 Mode 2
2ECh	V_CSR_INQ_7_3	Mode_3	[0-31]	CSR 32-bit offset for Format 7 Mode 3
2F0h	V_CSR_INQ_7_4	Mode_4	[0-31]	CSR 32-bit offset for Format 7 Mode 4
2F4h	V_CSR_INQ_7_5	Mode_5	[0-31]	CSR 32-bit offset for Format 7 Mode 5
2F8h	V_CSR_INQ_7_6	Mode_6	[0-31]	CSR 32-bit offset for Format 7 Mode 6
2FCh	V_CSR_INQ_7_7	Mode_7	[0-31]	CSR 32-bit offset for Format 7 Mode 7
300h	V_CSR_INQ_7_8	Mode_8	[0-31]	CSR 32-bit offset for Format 7 Mode 8
304h	V_CSR_INQ_7_9	Mode_9	[0-31]	CSR 32-bit offset for Format 7 Mode 9
308h	V_CSR_INQ_7_10	Mode_10	[0-31]	CSR 32-bit offset for Format 7 Mode 10
30Ch	V_CSR_INQ_7_11	Mode_11	[0-31]	CSR 32-bit offset for Format 7 Mode 11
310h	V_CSR_INQ_7_12	Mode_12	[0-31]	CSR 32-bit offset for Format 7 Mode 12
314h	V_CSR_INQ_7_13	Mode_13	[0-31]	CSR 32-bit offset for Format 7 Mode 13
318h	V_CSR_INQ_7_14	Mode_14	[0-31]	CSR 32-bit offset for Format 7 Mode 14

Offset	Name	Field	Bit	Description
31Ch	V_CSR_INQ_7_15	Mode_15	[0-31]	CSR 32-bit offset for Format 7 Mode 15
320h	V_CSR_INQ_7_16	Mode_16	[0-31]	CSR 32-bit offset for Format 7 Mode 16
324h	V_CSR_INQ_7_17	Mode_17	[0-31]	CSR 32-bit offset for Format 7 Mode 17
328h	V_CSR_INQ_7_18	Mode_18	[0-31]	CSR 32-bit offset for Format 7 Mode 18
32Ch	V_CSR_INQ_7_19	Mode_19	[0-31]	CSR 32-bit offset for Format 7 Mode 19
330h	V_CSR_INQ_7_20	Mode_20	[0-31]	CSR 32-bit offset for Format 7 Mode 20
334h	V_CSR_INQ_7_21	Mode_21	[0-31]	CSR 32-bit offset for Format 7 Mode 21
338h	V_CSR_INQ_7_22	Mode_22	[0-31]	CSR 32-bit offset for Format 7 Mode 22
33Ch	V_CSR_INQ_7_23	Mode_23	[0-31]	CSR 32-bit offset for Format 7 Mode 23
340h	V_CSR_INQ_7_24	Mode_24	[0-31]	CSR 32-bit offset for Format 7 Mode 24
344h	V_CSR_INQ_7_25	Mode_25	[0-31]	CSR 32-bit offset for Format 7 Mode 25
348h	V_CSR_INQ_7_26	Mode_26	[0-31]	CSR 32-bit offset for Format 7 Mode 26
34Ch	V_CSR_INQ_7_27	Mode_27	[0-31]	CSR 32-bit offset for Format 7 Mode 27
350h	V_CSR_INQ_7_28	Mode_28	[0-31]	CSR 32-bit offset for Format 7 Mode 28
354h	V_CSR_INQ_7_29	Mode_29	[0-31]	CSR 32-bit offset for Format 7 Mode 29
358h	V_CSR_INQ_7_30	Mode_30	[0-31]	CSR 32-bit offset for Format 7 Mode 30
35Ch	V_CSR_INQ_7_31	Mode_31	[0-31]	CSR 32-bit offset for Format 7 Mode 31

3 General Camera Operation

3.1 Memory Channel Registers

User Set 0 (or Memory channel 0) stores the factory default settings that can always be restored. Two additional user sets are provided for custom default settings. The camera initializes itself at power-up, or when explicitly reinitialized, using the contents of the last saved user set. Attempting to save user settings to the (read-only) factory default user set causes the camera to switch back to using the factory defaults during initialization.

The values of the following registers are saved in memory channels.

Register Name	Offset
CURRENT_FRAME_RATE	600h
CURRENT_VIDEO_MODE	604h
CURRENT_VIDEO_FORMAT	608h
CAMERA_POWER	610h
CUR_SAVE_CH	620h
BRIGHTNESS	800h
AUTO_EXPOSURE	804h
SHARPNESS	808h
WHITE_BALANCE	80Ch
HUE	810h
SATURATION	814h
GAMMA	818h
SHUTTER	81Ch
GAIN	820h
IRIS	824h
FOCUS	828h
TRIGGER_MODE	830h
TRIGGER_DELAY	834h
FRAME_RATE	83Ch
PAN	884h
TILT	888h
ABS_VAL_AUTO_EXPOSURE	908h
ABS_VAL_SHUTTER	918h
ABS_VAL_GAIN	928h
ABS_VAL_BRIGHTNESS	938h
ABS_VAL_GAMMA	948h
ABS_VAL_TRIGGER_DELAY	958h
ABS_VAL_FRAME_RATE	968h
IMAGE_DATA_FORMAT	1048h

Register Name	Offset
AUTO_EXPOSURE_RANGE	1088h
AUTO_SHUTTER_RANGE	1098h
AUTO_GAIN_RANGE	10A0h
GPIO_XTRA	1104h
SHUTTER_DELAY	1108h
GPIO_STRPAT_CTRL	110Ch
GPIO_CTRL_PIN_x	1110h, 1120h, 1130h, 1140h
GPIO_XTRA_PIN_x	1114h, 1124h, 1134h, 1144h
GPIO_STRPAT_MASK_PIN_x	1118h, 1128h, 1138h, 1148h
MIRROR_IMAGE_CTRL	1054h
FRAME_INFO	12F8h
FORMAT_7_IMAGE_POSITION	008h
FORMAT_7_IMAGE_SIZE	00Ch
FORMAT_7_COLOR_CODING_ID	010h
FORMAT_7_BYTE_PER_PACKET	044h
UDP_PORT	1F1Ch
DESTINATION_IP	1F34h
GVCP Configuration (includes Heartbeat Disable) (GigE Vision Bootstrap Register)	0954h (no offset)
Stream Channel Packet Size (GigE Vision Bootstrap Register)	0D04h (no offset)
Stream Channel Packet Delay (GigE Vision Bootstrap Register)	0D08h (no offset)
Heartbeat Timeout (GigE Vision Bootstrap Register)	0938h (no offset)

3.1.1 MEMORY_SAVE: 618h

All channels can be reset back to the original factory defaults by writing the value 0xDEAFBEEF to Memory_Save (ignores MEM_SAVE_CH).

Format:

Field	Bit	Description
Memory_Save	[0]	1 = Current status, modes, and values are saved to MEM_SAVE_CH (Self cleared)
	[1-31]	Reserved

3.1.2 MEM_SAVE_CH: 620h

Format:

Field	Bit	Description
Mem_Save_Ch	[0-3]	Specifies the write channel for Memory_Save command. Shall be >=0001 (0 is for factory default settings) See BASIC_FUNC_INQ register.
	[4-31]	Reserved

3.1.3 CUR_MEM_CH: 624h

Format:

Field	Bit	Description
Cur_Mem_Ch	[0-3]	Read: Reports the current memory channel number in use Write: Loads the camera status, modes and values from the specified memory channel
	[4-31]	Reserved

3.2 Device Information

Information about the camera 's hardware, status and monitoring is available.

Serial Number—This specifies the unique serial number of the camera.

Main Board Information—This specifies the type of camera (according to the main printed circuit board).

Voltage—This allows the user to access and monitor the input as well as several of the internal voltages of the cameras.

Current—This allows the user to access and monitor the current consumption of the camera.

Temperature—Allows the user to get the temperature of the camera board-level components. For cameras housed in a case, it is the ambient temperature within the case.

Camera Power—Allows the user to power up or power down the camera.

Pixel Clock Frequency—This specifies the current pixel clock frequency (in Hz) in IEEE-754 32-bit floating point format. The camera pixel clock defines an upper limit to the rate at which pixels can be read off the image sensor.

Horizontal Line Frequency—This specifies the current horizontal line frequency in Hz in IEEE-754 32-bit floating point format.

3.2.1 SERIAL_NUMBER: 1F20h

Format:

Field	Bit	Description
Serial_Number	[0-31]	Unique serial number of camera (read-only)

3.2.2 MAIN_BOARD_INFO: 1F24h

Format:

Field	Bit	Description
Major_Board_Design	[0-11]	0x6: Ladybug Head 0x7: Ladybug Base Unit 0x10: Flea 0x18: Dragonfly2 0x19: Flea2 0x1A: Firefly MV 0x1C: Bumblebee2 0x1F: Grasshopper 0x22: Grasshopper2 0x21: Flea2G-13S2 0x24: Flea2G-50S5 0x26: Chameleon 0x27: Grasshopper Express 0x29: Flea3 FireWire 14S3/20S4 0x2A: Flea3 FireWire 03S3 0x2B: Flea3 FireWire 03S1 0x2F: Flea3 GigE 14S3/20S4 0x32: Flea3 GigE 13S2 0x34: Flea3 USB 3.0 0x36: Zebra2 0x39: Flea3 GigE 03S2/08S2 0x3E: Flea3 GigE 50S5 0x3F: Flea3 GigE 28S4 0x40: Flea3 GigE 03S1 0x41 Grasshopper3 PGE/USB3 0x46 Blackfly PGE 0x4B Blackfly USB3 0x4C Chameleon3 USB3
Minor_Board_Rev	[12-15]	Internal use
Reserved	[16-31]	Reserved

3.2.3 VOLTAGE: 1A50h – 1A54h

Format:

Offset	Name	Field	Bit	Description
1A50h	VOLTAGE_LO_INQ	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-7]	Reserved
			[8-19]	Number of voltage registers supported
		-	[20-31]	Reserved
1A54h	VOLTAGE_HI_INQ		[0-31]	32-bit offset of the voltage CSRs, which report the current voltage in Volts using the 32-bit floating-point IEEE/REAL*4 format.

3.2.4 CURRENT: 1A58h – 1A5Ch

Format:

Offset	Name	Field	Bit	Description
1A58h	CURRENT_LO_INQ	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
			[1-7]	Reserved
			[8-19]	Number of current registers supported
			[20-31]	Reserved
1A5Ch	CURRENT_HI_INQ		[0-31]	32-bit offset of the current registers, which report the current in amps using the 32-bit floating-point IEEE/REAL*4 format.

3.2.5 TEMPERATURE: 82Ch

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-19]	Reserved
Value	[20-31]	Value. In Kelvin (0°C = 273.15K) in increments of one-tenth (0.1) of a Kelvin

3.2.6 CAMERA_POWER: 610h

Format:

Field	Bit	Description
Cam_Pwr_Ctrl	[0]	Read: 0: Camera is powered down, or in the process of powering up (i.e., bit will be zero until camera completely powered up (outside IIDC specification)), 1: Camera is powered up Write: 0: Begin power-down process, 1: Begin power-up process
	[1-30]	Reserved
Camera_Power_Status	[31]	Read only Read: the pending value of Cam_Pwr_Ctrl

3.2.7 PIXEL_CLOCK_FREQ: 1AF0h

Format:

Field	Bit	Description
Pixel_Clock_Freq	[0-31]	Pixel clock frequency in Hz (read-only).

3.2.8 HORIZONTAL_LINE_FREQ: 1AF4h

Format:

Field	Bit	Description
Horizontal_Line_Freq	[0-31]	Horizontal line frequency in Hz (read-only).

3.3 Camera Memory

3.3.1 DATA_FLASH_CTRL: 1240h

This register controls access to the camera's on-board flash memory. Each bit in the data flash is initially set to 1.

The user can transfer as much data as necessary to the offset address (1244h), then perform a single write to the control register to commit the data to flash. Any modified data is committed by writing to this register, or by accessing any other control register.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
Clean_Page	[6]	Read: 0: Page is dirty, 1: Page is clean Write: 0: No-op, 1: Write page to data flash
	[7]	Reserved
Page_Size	[8-19]	8 == 256 byte page 9 == 512 byte page
Num_Pages	[20-31]	11 == 2048 pages 13 == 8192 pages

3.3.2 DATA_FLASH_DATA: 1244h

This register provides the 32-bit offset to the start of where the data is stored in the flash memory.

Format:

Offset	Field	Bit	Description
1244h	DF_Data	[0-31]	32-bit offset to the start of data

3.3.3 IMAGE_RETRANSMIT: 634h

> **Note:** This register is for cameras supported by IIDC Specification v1.32 only. Cameras supported by IIDC Specification v1.31 should use IMAGE_RETRANSMIT: 12E8h (IIDC 1.31).

This register provides an interface to the camera's frame buffer functionality.

Transmitting buffered data is available when continuous shot is disabled. Either One shot or Multi shot can be used to transmit buffered data when *Transfer_Data_Select* = 1. Multi shot is used for transmitting one or more (as specified by *Count_Number*) buffered images. One shot is used for retransmission of the last image from the retransmit buffer.

Image data is stored in a circular image buffer when *Image_Buffer_Ctrl* = 1. If the circular buffer overflows, the oldest image in the buffer is overwritten.

Transmitted data is always stored in the retransmit buffer. If a last or previous image does not exist, (for example, an image has not been acquired since a video format or mode change), the camera still transmits an image from the retransmit buffer, but its contents are undefined.

The image buffer is initialized when *Image_Buffer_Ctr* is written to '1'. Changing the video format, video mode, image_size, or color_coding causes the image buffer to be initialized and *Max_Num_Images* to be updated.

Format:

Field	Bit	Description
Image_Buffer_Ctrl	[0]	Image Buffer On/Off Control 0: OFF, 1: ON
Transfer_Data_Select	[1]	Transfer data path 0: Live data, 1: Buffered image data Ignored if ISO_EN=1
	[2-7]	Reserved
Max_Num_Images	[8-19]	Maximum number of images that can be stored in the current video format. Must be greater than zero. This field is read only.
Number_of_Images	[20-31]	The number of images currently in buffer. This field is read only.

3.3.4 IMAGE_RETRANSMIT: 12E8h (IIDC 1.31)

Note: This register is for cameras supported by IIDC Specification v1.31 only. Cameras supported by IIDC Specification v1.32 should use IMAGE_RETRANSMIT: 634h.

This register provides an interface to the camera's frame buffer functionality. The user can cause images to accumulate in the frame buffer by enabling the HoldImg bit of register 12E8h. This effectively disables the transmission of images over the interface in favor of accumulating them in the frame buffer. The user is then required to use the remaining elements of the interface to cause the transmission of the images.

The buffer system is circular in nature, storing only the most recent image data allowed by the buffer size. The number of images that this amounts to depends on the currently configured image size.

See ONE_SHOT/MULTI_SHOT: 61Ch for information on transmitting images.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
Reserved	[1-5]	Reserved
HoldImg	[6]	Store images to frame buffer rather than transmitting 0: Off 1: On
Reserved	[7-15]	Reserved
BufferSize	[16-23]	Maximum number of images in the current configuration.

Field	Bit	Description
NumOfImages	[24-31]	Read: Number of images currently in buffer. Write: When HoldImg is enabled, transmits a single image and deletes the specified number of images from the buffer.

3.4 Firmware Information

3.4.1 FIRMWARE_VERSION: 1F60h

This register contains the version information for the currently loaded camera firmware.

Format:

Field	Bit	Description
Major	[0-7]	Major revision number
Minor	[8-15]	Minor revision number
Type	[16-19]	Type of release: 0: Alpha 1: Beta 2: Release Candidate 3: Release
Revision	[20-31]	Revision number

3.4.2 FIRMWARE_BUILD_DATE: 1F64h

Format:

Field	Bit	Description
Build_Date	[0-31]	Date the current firmware was built in Unix time format (read-only)

3.4.3 FIRMWARE_DESCRIPTION: 1F68-1F7Ch

Null padded, big-endian string describing the currently loaded version of firmware.

4 Input/Output Control

4.1 General Purpose Input/Output (GPIO)

6-pin Blackfly®:

The camera is equipped with a 6-pin GPIO connector on the back of the case. The connector is a Hirose HR10A-7R-6PB, the mating connector is a Hirose HR10A-7P-6S(73).

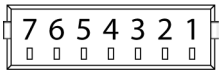
Blackfly

Diagram	Color	Pin	Function	Description
	Green	1	Power	+12 V DC Camera Power
	Black	2	Opto Input 1	Opto-isolated input
	Red	3	NC / +3.3 V / GPIO	+3.3 V output. Current 120 mA (nominal) Firmware enabled / Non-isolated I/O
	White	4	Opto Output 1	Opto-isolated output
	Blue	5	Opto GND	Ground for opto-isolated I/O, not connected to camera ground
	Brown	6	GND	DC camera power ground

7- pin Chameleon® and Firefly®MV:

The camera is equipped with a 7-pin GPIO connector on the back of the case. The connector is made by JST (Mfg P/N: BM07B-SRSS-TB). The Development Kit contents include a pre-wired female connector; refer to the diagram below for wire color-coding.

Chameleon, FireflyMV

Diagram	Color	Pin	Function	Description
TOP 	White	1	V_{EXT}	Allows the camera to be powered externally
	Red	2	+3.3V	Power external circuitry up to a total of 150 mA
	Green	3	IO0	Input/Output (Default Trigger_Scr)
	Green	4	IO1	Input/Output
	Grey	5	IO2	Input/Output/RS232 Transmit (TX)
	Grey	6	IO3	Input/Output/RS232 Receive (RX)
	Black	7	GND	Ground

8-pin Flea®3, Grasshopper®3:

The camera has an 8-pin GPIO connector on the back of the case; refer to the diagram below for wire color-coding. The connector is a Hirose HR25 8 pin connector with part number: HR25-7TR-8SA. The male connector is part number: HR25-7TP-8P.

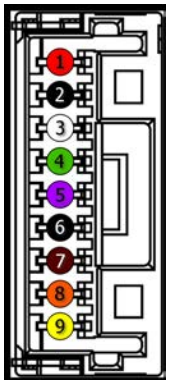
Flea3, Grasshopper3

Diagram	Color	Pin	Function	Description
	Black	1	I0	Opto-isolated input (default Trigger in)
	White	2	O1	Opto-isolated output
	Red	3	IO2	Input/Output/serial transmit (TX)
	Green	4	IO3	Input/Output/serial receive (RX)
	Brown	5	GND	Ground for bi-directional IO, V_{EXT}, +3.3 V pins
	Blue	6	OPTO_GND	Ground for opto-isolated IO pins
	Orange	7	V_{EXT}	Allows the camera to be powered externally
	Yellow	8	+3.3 V	Power external circuitry up to 150 mA

9-pin Chameleon®3:

The camera has a 9-pin GPIO connector on the back of the case; refer to the diagram below for wire color-coding. The header connector is JST part number BM09B-NSHSS-TBT and the wire plug connector is JST part number NSHR-09V-S. The wire contacts are SSHL-003T-P0.2.

Chameleon3

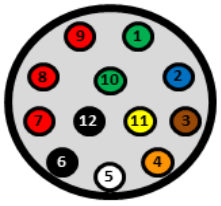
Diagram	Color	Pin	Function	Description
	Red	1	V_{EXT}	Allows the camera to be powered externally 5 - 24 VDC
	Black	2	GND	Ground for Input/Output, V_{EXT}, +3.3 V pins
	White	3	+3.3 V	Power external circuitry fused at 150 mA maximum
	Green	4	GPIO3 / Line3	Input/Output
	Purple	5	GPIO2 / Line2	Input/Output
	Black	6	GND	Ground for Input/Output, V_{EXT}, +3.3 V pins
	Brown	7	OPTO_GND	Ground for opto-isolated IO pins
	Orange	8	OPTO_OUT / Line1	Opto-isolated output
	Yellow	9	OPTO_IN / Line0	Opto-isolated input

Ladybug®5:

The camera has an 12-pin GPIO connector on the bottom of the case; refer to the diagram below for wire color-coding. The GPIO is a Hirose waterproof 12-pin female connector (Mfg P/N:LF10WBP-12SD).

The camera comes with a 6-meter power cable and wiring harness with a Hirose 12-pin male connector (Mfg P/N: LF10WBP-12P).

Ladybug5

Diagram	Color	Pin	Function	Description
	Green	1	OPTO_GND	Ground for opto-isolated IO pins
	Blue	2	I0	Opto-isolated input (default Trigger in)
	Brown	3	O1	Opto-isolated output
	Orange	4	IO2	Input/Output
	White	5	+3.3 V	Power external circuitry up to 150 mA
	Black	6	GND	Ground for bi-directional IO, V_{EXT}, +3.3 V pins
	Red	7	V_{EXT}	Allows the camera to be powered externally
	Red	8	V_{EXT}	Allows the camera to be powered externally
	Red	9	V_{EXT}	Allows the camera to be powered externally
	Green	10	OPTO_GND	Ground for opto-isolated IO pins
	Yellow	11	IO3	Input/Output
	Black	12	GND	Ground for bi-directional IO, V_{EXT}, +3.3 V pins

4.2 GPIO Modes

4.2.1 GPIO Mode 0: Input

When a GPIO pin is put into GPIO Mode 0 it is configured to accept external trigger signals.

4.2.2 GPIO Mode 1: Output

When a GPIO pin is put into GPIO Mode 1 it is configured to send output signals.

Warning! Do **not** connect power to a pin configured as an output (effectively connecting two outputs to each other). Doing so can cause damage to camera electronics.

4.2.3 GPIO Mode 2: Asynchronous (External) Trigger

When a GPIO pin is put into GPIO Mode 2, and an external trigger mode is enabled (which disables isochronous data transmission), the camera can be asynchronously triggered to grab an image by sending a voltage transition to the pin.

4.2.4 GPIO Mode 3: Strobe

A GPIO pin in GPIO Mode 3 outputs a voltage pulse of fixed delay, either relative to the start of integration (default) or relative to the time of an asynchronous trigger. A GPIO pin in this mode can be configured to output a variable strobe pattern.

4.2.5 GPIO Mode 4: Pulse Width Modulation (PWM)

When a GPIO pin is set to GPIO Mode 4, the pin outputs a specified number of pulses with programmable high and low duration..

4.3 GPIO_CTRL_PIN: 1110h-1140h

These registers provide control over the GPIO pins.

Pin	Register	
0	GPIO_CTRL_PIN_0	1110h
1	GPIO_CTRL_PIN_1	1120h
2	GPIO_CTRL_PIN_2	1130h
3	GPIO_CTRL_PIN_3	1140h

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-11]	Reserved
Pin_Mode	[12-15]	Current GPIO Mode: 0: Input 1: Output 2: Asynchronous Trigger 3: Strobe 4: Pulse width modulation (PWM)
	[16-30]	For Modes 0, 1, and 2: Reserved For Mode 4 (PWM:) see below
Data	[31]	For Modes 0, 1, and 2: Data field 0 = 0 V (falling edge), 1 = +3.3 V (rising edge) For Mode 4 (PWM): see below
Pwm_Count	[16-23]	Number of PWM pulses Read: The current count; counts down the remaining pulses. After reaching zero, the count does not automatically reset to the previously-written value. Write: Writing the number of pulses starts the PWM. Write 0xFF for infinite pulses. (Requires write of 0x00 before writing a different value.)
	[24]	Reserved
En_Pin	[25-27]	The GPIO pin to be used as a PWM enable i.e. the PWM continues as long as the En_Pin is held in a certain state (high or low).
	[28]	Reserved
Disable_Pol	[29]	Polarity of the PWM enable pin (En_Pin) that will disable the PWM. If this bit is 0, the PWM is disabled when the PWM enable pin goes low.
En_En	[30]	0: Disable enable pin (En_Pin) functionality 1: Enable En_Pin functionality

Field	Bit	Description
Pwm_Pol	[31]	Polarity of the PWM signal 0: Low, 1: High

4.4 GPIO_XTRA_PIN: 1114h-1144h

These registers contain mode specific data for the GPIO pins. Units are ticks of a 1.024MHz clock.

Pin	Register	
0	GPIO_XTRA_PIN_0	1114h
1	GPIO_XTRA_PIN_1	1124h
2	GPIO_XTRA_PIN_2	1134h
3	GPIO_XTRA_PIN_3	1144h

Format:

Field	Bit	Description
Mode_Specific_1	[0-15]	GPIO_MODE_4: Low period of PWM pulse (if Pwm_Pol = 0)
Mode_Specific_2	[16-31]	GPIO_MODE_4: High period of PWM pulse (if Pwm_Pol = 0)

4.5 GPIO_CONTROL: 1100h

This register provides status information about the camera's GPIO pins.

Note: Opto-isolated input pins with pull-up resistors report a value of '1' when unconnected. Consult your camera's Technical Reference manual for GPIO pinout details.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-11]	Reserved
Pin_Count	[12-15]	Number of available GPIO pins
	[16-27]	Reserved
Value_3	[28]	Value of IO3 0: Voltage low; 1: Voltage high
Value_2	[29]	Value of IO2 0: Voltage low; 1: Voltage high
Value_1	[30]	Value of IO1 0: Voltage low; 1: Voltage high
Value_0	[31]	Value of IO0 0: Voltage low; 1: Voltage high

4.5.1 PIO_OUTPUT: 11F0h (IIDC v1.31)

This section is for cameras using the *IIDC 1394-based Digital Camera (DCAM) Specification* version 1.31. This does not apply to cameras using version 1.32.

Format

Field	Bit	Description
IO0_Status	[0]	State (voltage level) of the IO Pin 0 0: Low, 1: High
IO1_Status	[1]	State (voltage level) of the IO Pin 1 0: Low, 1: High
IO2_Status	[2]	State (voltage level) of the IO Pin 2 0: Low, 1: High
IO3_Status	[3]	State (voltage level) of the IO Pin 3 0: Low, 1: High
	[4-31]	Reserved

4.6 GPIO_STRPAT_CTRL: 110Ch

This register provides control over a shared 4-bit counter with programmable period. When the *Current_Count* equals N a GPIO pin will only output a strobe pulse if bit[N] of the GPIO_STRPAT_MASK_PIN_x register's *Enable_Pin* field is set to '1'.

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-18]	Reserved
Count_Period	[19-23]	Controls the period of the strobe pattern Valid values: 1..16
	[24-27]	Reserved
Current_Count	[28-31]	Read-only The value of the bit index defined in GPIO_x_STRPAT_MASK that will be used during the next image's strobe. *Current_Count* increments at the same time as the strobe start signal occurs.

4.7 GPIO_STRPAT_MASK_PIN: 1118h-1148h

These registers define the actual strobe pattern to be implemented by GPIO pins in conjunction with the *Count_Period* defined in GPIO_STRPAT_CTRL register 110Ch.

For example, if *Count_Period* is set to '3', bits 16-18 of the *Enable_Mask* can be used to define a strobe pattern. An example strobe pattern might be bit 16=0, bit 17=0, and bit 18=1, which will cause a strobe to occur every three frames (when the *Current_Count* is equal to 2).

Pin	Register	
0	GPIO_STRPAT_MASK_PIN_0	1118h
1	GPIO_STRPAT_MASK_PIN_1	1128h

Pin	Register	
2	GPIO_STRPAT_MASK_PIN_2	1138h
3	GPIO_STRPAT_MASK_PIN_3	1148h

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-15]	Reserved
Enable_Mask	[16-31]	Bit field representing the strobe pattern used in conjunction with *Count_Period* in GPIO_STRPAT_CTRL 0: Do not output a strobe, 1: Output a strobe

4.8 Strobe Output Registers

Note: To calculate the base address for an offset CSR:

1. Query the offset inquiry register.
2. Multiple the value by 4. (The value is a 32-bit offset.)
3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

Format:

Offset	Name	Field	Bit	Description
48Ch	STROBE_OUTPUT_CSR_INQ	Strobe_Output_Quadlet_Offset	[0-31]	32-bit offset of the Strobe output signal CSRs from the base address of initial register space
Base + 0h	STROBE_CTRL_INQ	Strobe_0_Inq	[0]	Presence of strobe 0 signal
		Strobe_1_Inq	[1]	Presence of strobe 1 signal
		Strobe_2_Inq	[2]	Presence of strobe 2 signal
		Strobe_3_Inq	[3]	Presence of strobe 3 signal
		-	[4-31]	Reserved

Offset	Name	Field	Bit	Description
Base + 100h	STROBE_ 0_INQ	Presence_ Inq	[0]	Presence of this feature
			[1-3]	Reserved
		ReadOut_ Inq	[4]	Ability to read the value of this feature
		On_Off_Inq	[5]	Ability to switch feature ON and OFF
		Polarity_Inq	[6]	Ability to change signal polarity
			[7]	Reserved
		Min_Value	[8-19]	Minimum value for this feature control
		Max_Value	[20-31]	Maximum value for this feature control
Base + 104h	STROBE_ 1_INQ	Same definition as Strobe_0_Inq		
Base + 108h	STROBE_ 2_INQ	Same definition as Strobe_0_Inq		
Base + 10Ch	STROBE_ 3_INQ	Same definition as Strobe_0_Inq		
Base + 200h	STROBE_ 0_CNT	Presence_ Inq	[0]	Presence of this feature 0: Not Available, 1: Available
			[1-5]	Reserved
		On_Off	[6]	Read: read a status Write: ON or OFF this function 0: OFF, 1: ON If this bit = 0, other fields will be read only. **Note:** When ON, strobe signals continue to output after the camera stops streaming images. To stop strobe output, this bit must be explicitly turned OFF.
		Signal_ Polarity	[7]	Select signal polarity If Polarity_Inq = 1: Read to get strobe output polarity Write to change strobe output polarity If Polarity_Inq = 0, then Read only 0: Low active output, 1: High active output
		Delay_Value	[8-19]	Delay after start of exposure until the strobe signal asserts
		Duration_ Value	[20-31]	Duration of the strobe signal A value of 0 means de-assert at the end of exposure, if required.

Offset	Name	Field	Bit	Description
Base + 204h	STROBE_ 1_CNT	Same definition as Strobe_0_Cnt		Default Settings: [0] = 1 [6] = 1 [7] = 0 [8-19] = 0 [20-31] = 0
Base + 208h	STROBE_ 2_CNT	Same definition as Strobe_0_Cnt		
Base + 20Ch	STROBE_ 3_CNT	Same definition as Strobe_0_Cnt		

4.9 Serial Input/Output Registers

This section describes the control and inquiry registers for the serial input/output (SIO) control functionality.

Note: To calculate the base address for an offset CSR:

1. Query the offset inquiry register.
2. Multiple the value by 4. (The value is a 32-bit offset.)
3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

Offset	Name	Field	Bit	Description
488h	SIO_ CONTROL_ CSR_INQ	SIO_ Control_ Quadlet_ Offset	[0-31]	32-bit offset of the SIO CSRs from the base address of initial register space
Base + 0h	SERIAL_ MODE_REG	Baud_ Rate	[0-7]	*Baud rate setting* Read: Get current baud rate Write: Set baud rate 0: 300 bps 1: 600 bps 2: 1200 bps 3: 2400 bps 4: 4800 bps 5: 9600 bps 6: 19200 bps 7: 38400 bps 8: 57600 bps 9: 115200 bps 10: 230400 bps Other values reserved

Offset	Name	Field	Bit	Description
		Char_ Length	[8-15]	Character length setting Read: Get data length Write: Set data length (must not be 0) 7: 7 bits, 8: 8 bits Other values reserved
		Parity	[16-17]	*Parity setting* Read: Get current parity Write: Set parity 0: None, 1: Odd, 2: Even
		Stop_Bit	[18-19]	*Stop bits* Read: Get current stop bit Write: Set stop bit 0: 1, 1: 1.5, 2: 2
			[20-23]	Reserved
		Buffer_ Size_Inq	[24-31]	*Buffer Size (Read-Only)* This field indicates the maximum size of the receive/transmit data buffer. If this value=1, *Buffer_Status_Control* and *SIO_Data_Register* characters 1-3 should be ignored.
Base + 4h	SERIAL_ CONTROL_ REG	RE	[0]	Receive enable Indicates if the camera's ability to receive data has been enabled. Enabling this register causes the receive capability to be immediately started. Disabling this register causes the data in the buffer to be flushed. Read: Current status Write: 0 Disable, 1: Enable
		TE	[1]	*Transmit enable* Indicates if the camera's ability to transmit data has been enabled. Enabling this register causes the transmit capability to be immediately started. Disabling this register causes data transmission to stop immediately, and any pending data is discarded. Read: Current status Write: 0: Disable, 1: Enable
		-	[2-7]	Reserved
	SERIAL_ STATUS_REG	TDRD	[8]	*Transmit data buffer ready (read only)* Indicates if the transmit buffer is ready to receive data from the user. It will be in the Ready state as long as *TBUF_ST* != 0 and *TE* is enabled. Read only 0: Not ready, 1: Ready
		-	[9]	Reserved

Offset	Name	Field	Bit	Description
		RDRD	[10]	*Receive data buffer ready (read only)* Indicates if the receive buffer is ready to be read by the user. It will be in the Ready state as long as *RBUF_ST* != 0 and *RE* is enabled. Read only 0: Not ready, 1: Ready
		-	[11]	Reserved
		ORER	[12]	*Receive buffer over run error* Read: Current status Write: 0: Clear flag, 1: Ignored
		FER	[13]	*Receive data framing error* Read: Current status Write: 0: Clear flag, 1: Ignored
		PER	[14]	*Receive data parity error* Read: Current status Write: 0: Clear flag, 1: Ignored
		-	[15-31]	Reserved
Base + 8h	RECEIVE_ BUFFER_ STATUS_ CONTROL	RBUF_ST	[0-8]	*SIO receive buffer status* Indicates the number of bytes that have arrived at the camera but have yet to be queued to be read. Read: Valid data size of current receive buffer Write: Ignored
		RBUF_ CNT	[8-15]	*SIO receive buffer control* Indicates the number of bytes that are ready to be read. Read: Remaining data size for read Write: Set input data size
		-	[16-31]	Reserved
Base + Ch	TRANSMIT_ BUFFER_ STATUS_ CONTROL	TBUF_ST	[0-8]	*SIO output buffer status* Indicates the minimum number of free bytes available to be filled in the transmit buffer. It will count down as bytes are written to any of the SIO_DATA_REGISTERs starting at 2100h. It will count up as bytes are actually transmitted after a write to *TBUF_CNT*. Although its maximum value is 255, the actual amount of available buffer space may be larger. Read: Available data space of transmit buffer Write: Ignored

Offset	Name	Field	Bit	Description
		TBUF_CNT	[8-15]	*SIO output buffer control* Indicates the number of bytes that have been stored since it was last written to. Writing any value to *TBUF_CNT* will cause it to go to 0. Writing a number less than its value will cause that many bytes to be transmitted and the rest thrown away. Writing a number greater than its value will cause that many bytes to be written - its value being valid and the remainder being padding. Read: Written data size to buffer Write: Set output data size for transmit.
		-	[16-31]	Reserved
Base + 100h	SIO_DATA_REGISTER	Char_0	[0-7]	*Character_0* Read: Read character from receive buffer. Padding data if data is not available. Write: Write character to transmit buffer. Padding data if data is invalid.
		Char_1	[8-16]	*Character_1* Read: Read character from receive buffer+1. Padding data if data is not available. Write: Write character to transmit buffer+1. Padding data if data is invalid.
		Char_2	[17-23]	*Character_2* Read: Read character from receive buffer+2. Padding data if data is not available. Write: Write character to transmit buffer+2. Padding data if data is invalid.
		Char_3	[24-31]	*Character_3* Read: Read character from receive buffer+3. Padding data if data is not available. Write: Write character to transmit buffer+3. Padding data if data is invalid.
Base + 104h : Base + 1FFh	SIO_DATA_REGISTER_ALIAS		[0-31]	Alias SIO_Data_Register area for block transfer.

4.10 DEBOUNCER_CTRL

These registers provide control over the debouncer.

> **Note:** The DEBOUNCER_INQ registers allows for the presence of the debouncer on all eight GPIO pins. However, the debouncer feature only works on GPIO input pins: GPIO0, GPIO2, and GPIO3.

4.10.1 DEBOUNCER_INQ: 11fch

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Debouncer_0_Inq	[1]	Presence of the debouncer on GPIO_0
Debouncer_1_Inq	[2]	Presence of the debouncer on GPIO_1
Debouncer_2_Inq	[3]	Presence of the debouncer on GPIO_2
Debouncer_3_Inq	[4]	Presence of the debouncer on GPIO_3
Debouncer_4_Inq	[5]	Presence of the debouncer on GPIO_4
Debouncer_5_Inq	[6]	Presence of the debouncer on GPIO_5
Debouncer_6_Inq	[7]	Presence of the debouncer on GPIO_6
Debouncer_7_Inq	[8]	Presence of the debouncer on GPIO_7
	[9-10]	Reserved
Min_Value	[11]	Minimum value for debouncer control in microseconds. Must be greater than or equal to 1 microsecond.
Max_Value	[12-31]	Maximum value for debouncer control in microseconds. Must be less than or equal to 1 second.

4.10.2 DEBOUNCER_X_CTRL: 111ch – 118ch

Register	
DEBOUNCER_0_CTRL	111ch
DEBOUNCER_1_CTRL	112ch
DEBOUNCER_2_CTRL	113ch
DEBOUNCER_3_CTRL	114ch
DEBOUNCER_4_CTRL	115ch
DEBOUNCER_5_CTRL	116ch
DEBOUNCER_6_CTRL	117ch
DEBOUNCER_7_CTRL	118ch

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
On_Off	[6]	Read: read a status Write: ON or OFF this function 0 = OFF; 1 = ON If this bit = 0, other fields will be read only.
	[7-11]	Reserved
Debouncer_Value	[12-31]	Debouncer value in microseconds. When Debounce_Value = 0 or On_Off is set to OFF, the camera defaults to using a value of 16 ticks of the current pixel clock.

4.11 OUTPUT_VOLTAGE_ENABLE: 1900h

This register is for the Blackfly camera only.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-30]	Reserved
ON_OFF	[31]	Enable or disable 3.3 V output on Blackfly GPIO pin 3. 0: Off, 1: On Default value is 0.

5 Video Format, Mode, and Frame Rate Settings

The following settings control the video format and mode of the camera.

Frame Rate—This provides control over the frame rate of the camera. When this feature is in auto mode, exposure time is limited by the frame rate value dynamically, which is determined by the Current Frame Rate. When this feature is in manual mode, the actual frame interval (time between individual image acquisitions) is fixed by the frame rate value. The available frame rate range depends on the current video format and/or video mode.

This is set to OFF when the camera is operating in asynchronous trigger mode.

Current Frame Rate—Allows the user to query and modify the current frame rate of the camera.

Current Video Mode—Allows the user to query and modify the current video mode of the camera.

Current Video Format—Allows the user to query and modify the current video format of the camera. Note: GigE Vision cameras only operate in Format 7.

5.1 FRAME_RATE: 83Ch

Note: Formulas for converting the fixed point (relative) values to floating point (absolute) values are not provided. Users wishing to work with real-world values should refer to Absolute Value CSRs.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Abs_Control	[1]	Absolute value control 0: Control in the Value field, 1: Control in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically only once) Read: 0: Not in operation, 1: In operation Write: 1: Begin to work (self-cleared after operation) If A_M_Mode = 1, this bit is ignored

Field	Bit	Description
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: read a current mode Write: set the mode 0: Manual, 1: Automatic
	[8-19]	Reserved
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.

5.2 CURRENT_FRAME_RATE: 600h

Format:

Field	Bit	Description
Cur_V_Frm_Rate	[0-2]	Current frame rate FrameRate_0 .. FrameRate_7
	[3-31]	Reserved.

5.3 CURRENT_VIDEO_MODE: 604h

Format:

Field	Bit	Description
Cur_V_Mode	[0-3]	Current video mode Mode_0 .. Mode_8
	[4-31]	Reserved.

5.4 CURRENT_VIDEO_FORMAT: 608h

Format:

Field	Bit	Description
Cur_V_Format	[0-2]	Current video format Format_0 .. Format_7 ***Note***: GigE Vision cameras operate only in Format 7 mode.
	[3-31]	Reserved.

5.5 FORMAT_7_RESIZE_INQ: 1AC8h

This register reports all internal camera processes being used to generate images in the current Format 7 video mode. For example, users can read this register to determine if pixel binning and/or subsampling is being used to achieve a non-standard custom image size.

This register is read-only.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-7]	Reserved
Num_Cols	[8-11]	Number of columns being binned/subsampled, minus 1 (e.g., if combining 4 columns together, this register will report a value of 3)
Num_Rows	[12-15]	Number of rows binned/subsampled, minus 1 (e.g., if combining 4 columns together, this register will report a value of 3)
	[16-23]	Reserved
V_Pre_Color	[24]	Vertical subsampling/downsampling performed before color processing 0: Off, 1: On
H_Pre_Color	[25]	Horizontal subsampling/downsampling performed before color processing 0: Off, 1: On
V_Post_Color	[26]	Vertical subsampling/downsampling performed after color processing 0: Off, 1: On
H_Post_Color	[27]	Horizontal subsampling/downsampling performed after color processing 0: Off, 1: On
V_Bin	[28]	Standard vertical binning (addition of adjacent lines within horizontal shift register) 0: Off, 1: On
H_Bin	[29]	Standard horizontal binning (addition of adjacent lines within horizontal shift register) 0: Off, 1: On
V_Bayer_Bin	[30]	Vertical bayer binning (addition of adjacent even/odd lines within the interline transfer buffer) 0: Off, 1: On
H_Bayer_Bin	[31]	Horizontal bayer binning (addition of adjacent even/odd columns within the horizontal shift register) 0: Off, 1: On

5.6 Inquiry Registers for Custom Video Mode (Format 7) Offset Addresses

The following set of registers indicates the locations of the custom video mode (Format 7) base registers. These offsets are relative to the base offset 0xFFFF F0F0 0000.

Table 5.1: Custom Video Mode (Format 7) Inquiry Register Offset Addresses

Offset	Name	Field	Bit	Description
2E0h	V_CSR_INQ_7_0	Mode_0	[0-31]	32-bit offset for Format 7 Mode 0
2E4h	V_CSR_INQ_7_1	Mode_1	[0-31]	32-bit offset for Format 7 Mode 1
2E8h	V_CSR_INQ_7_2	Mode_2	[0-31]	32-bit offset for Format 7 Mode 2
2ECh	V_CSR_INQ_7_3	Mode_3	[0-31]	32-bit offset for Format 7 Mode 3
2F0h	V_CSR_INQ_7_4	Mode_4	[0-31]	32-bit offset for Format 7 Mode 4
2F4h	V_CSR_INQ_7_5	Mode_5	[0-31]	32-bit offset for Format 7 Mode 5
2F8h	V_CSR_INQ_7_6	Mode_6	[0-31]	32-bit offset for Format 7 Mode 6
2FCh	V_CSR_INQ_7_7	Mode_7	[0-31]	32-bit offset for Format 7 Mode 7

Offset	Name	Field	Bit	Description
300h	V_CSR_INQ_7_8	Mode_8	[0-31]	32-bit offset for Format 7 Mode 8

Note: To calculate the base address for an offset CSR:

1. Query the offset inquiry register.
2. Multiple the value by 4. (The value is a 32-bit offset.)
3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

5.6.1 Image Size and Position

These registers are inquiry registers for maximum image size and unit size, and to determine an area of required data.

Format:

Address	Name	Field	Bit	Description
Base + 000h	MAX_IMAGE_SIZE_INQ	Hmax	[0-15]	Maximum horizontal pixel number Hmax = Hunit * n = Hposunit*n3 (n, n3 are integers)
		Vmax	[16-31]	Maximum vertical pixel number Vmax = Vunit * m = Vposunit*m3 (m, m3 are integers)
Base + 004h	UNIT_SIZE_INQ	Hunit	[0-15]	Horizontal unit pixel number
		Vunit	[16-31]	Vertical unit pixel number
Base + 04Ch	UNIT_POSITION_INQ	Hposunit	[0-15]	Horizontal unit pixel number for position If read value of Hposunit is 0, Hposunit = Hunit for IIDC 1.20 compatibility.
		Vposunit	[16-31]	Vertical unit number for position If read value of Vposunit is 0, Vposunit = Vunit for IIDC 1.20 compatibility.
Base + 008h	IMAGE_POSITION	Left	[0-15]	Left position of requested image region (pixels) Left = Hposunit * n1 Left + Width <= Hmax
		Top	[16-31]	Top position of requested image region (pixels) Top = Vposunit * m1 Top + Height <= Vmax
Base + 00Ch	IMAGE_SIZE	Width	[0-15]	Width of requested image region (pixels) Width = Hunit * n2
		Height	[16-31]	Height of requested image region (pixels) Height = Vunit * m2 (n1, n2, m1, m2 are integers)

5.6.2 COLOR_CODING_ID and COLOR_CODING_INQ

The COLOR_CODING_INQ register describes the color-coding (pixel format) capability of the system. Each coding scheme has its own ID number. The required color-coding scheme must be set to COLOR_CODING_ID register as the ID number.

Format:

Address	Name	Field	Bit	Description	ID
Base + 010h	COLOR_ CODING_ID	Coding_ID	[0-7]	Color coding ID from COLOR_CODING_INQ register	N/A
			[8-31]	Reserved	N/A
Base + 014h	COLOR_ CODING_INQ	Mono8	[0]	Y only. Y=8bits, non compressed	0
		4:1:1 YUV8	[1]	4:1:1, Y=U=V= 8bits, non compressed	1
		4:2:2 YUV8	[2]	4:2:2, Y=U=V=8bits, non compressed	2
		4:4:4 YUV8	[3]	4:4:4, Y=U=V=8bits, non compressed	3
		RGB8	[4]	R=G=B=8bits, non compressed	4
		Mono16	[5]	Y only, Y=16bits, non compressed	5
		RGB16	[6]	R=G=B=16bits, non compressed	6
		Signed Mono16	[7]	Y only, Y=16 bits, non compressed (signed integer)	7
		Signed RGB16	[8]	R=G=B=16 bits, non compressed (signed integer)	8
		Raw8	[9]	Raw data output of color filter sensor, 8 bits	9
		Raw16	[10]	Raw data output of color filter sensor, 16 bits	10
		Mono12	[11]	Y only. Y=12 bits, non compressed	
		Raw12	[12]	Raw data output of color filter sensor, 12 bits	
			[13-31]	Reserved	11-31
Base + 030h	COLOR_ CODING_INQ		[0-30]	Reserved	
		JPEG+YUV422	[31]	4:2:2, Y=U=V=8bits, JPEG-compressed	255

5.6.3 PACKET_PARA_INQ, BYTE_PER_PACKET, and PACKET_PER_FRAME

If the *Presence* bit in the VALUE_SETTING register (page 46) is zero, values of these fields will be updated by writing the new value to the IMAGE_POSITION, IMAGE_SIZE (page 44) and COLOR_CODING_ID (page 44) registers with the value of the ISO_Speed register(page 52).

First, the ISO_Speed register must be written. Then the IMAGE_POSITION, IMAGE_SIZE and COLOR_CODING_ID registers should be updated.

If the *Presence* bit in the VALUE_SETTING register is one, the values of these fields will be updated by writing one to the *Setting_1* bit in the VALUE_SETTING register. If the *ErrorFlag_1* bit is zero after the *Setting_1* bit returns to zero, the values of these fields are valid.

Format:

Address	Name	Field	Bit	Description
Base + 034h	PIXEL_NUMBER_ INQ	PixelPerFrame	[0-31]	Total number of pixels in the required image area
Base + 038h	TOTAL_BYTES_ HI_INQ	BytesPerFrameHi	[0-31]	Higher 32-bits of total bytes of image data per frame
Base + 03Ch	TOTAL_BYTES_ LO_INQ	BytesPerFrameLo	[0-31]	Lower 32-bits of total bytes of image data per frame

Address	Name	Field	Bit	Description
Base + 040h	PACKET_PARA_INQ	UnitBytePerPacket	[0-15]	Minimum bytes per packet; packet sizes must be multiples of the minimum
		MaxBytePerPacket	[16-31]	Maximum bytes per packet
Base + 044h	BYTE_PER_PACKET	BytePerPacket	[0-15]	Packet size. This value determines the real packet size and transmission speed for one frame image. BytePerPacket = UnitBytePerPacket * n BytePerPacket <= MaxBytePerPacket If BytePerPacket * n != Bytes Per Frame‡, you must use padding. (n is an integer)
		RecBytePerPacket	[16-31]	Recommended bytes per packet. If this value is zero, ignore this field.
Base + 048h	PACKET_PER_FRAME_INQ	PacketPerFrame	[0-31]	Number of packets per frame. Updated after BytePerPacket is written. Total number of bytes of transmission data per one frame = BytePerPacket * PacketPerFrame Number of bytes of padding = BytePerPacket * PacketPerFrame - Bytes Per Frame‡. The receiver must ignore the above padding in the last packet of each frame.
‡Example: Bytes Per Frame = Resolution Size * 1 byte per pixel = 640 * 480 = 307200 bytes per frame				

5.6.4 FRAME_INTERVAL_INQ

Format:

Address	Name	Field	Bit	Description
Base + 050h	FRAME_INTERVAL_INQ	FrameInterval	[0-31]	Current frame interval (seconds) based on the current camera conditions, including exposure time. The reciprocal value of this (1 / FrameInterval) is the frame rate of the camera. IEEE/REAL*4 floating-point value (see *Determining Absolute Value Register Values* If 0, the camera can't report the value and it should be ignored.

5.6.5 VALUE_SETTING

The purpose of the *Setting_1* bit is for updating the TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_PACKET (page 45) registers. If one of the values in the IMAGE_POSITION, IMAGE_SIZE (page 44) COLOR_CODING_ID (page 44) and ISO_SPEED (page 52) registers is changed, the *Setting_1* bit must be set to 1.

Format:

Address	Name	Field	Bit	Description
Base + 07Ch	VALUE_ SETTING	Presence	[0]	If this bit is 1, Setting_1 , ErrorFlag_1 and ErrorFlag_2 fields are valid. This bit is read only.
		Setting_1	[1]	If writing "1" to this bit, IMAGE_POSITION, IMAGE_SIZE, COLOR_CODING_ID and ISO_Speed register value will be reflected in PIXEL_NUMBER_INQ, TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_ PACKET registers. This bit is self-cleared.
			[2-7]	Reserved
		ErrorFlag_ 1	[8]	Indicates whether the current combination of the values of IMAGE_POSITION, IMAGE_SIZE, COLOR_CODING_ID and ISO_ Speed registers is valid or not. 0: no error, 1: error This flag will be updated every time Setting_1 bit returns to "0" from "1".
		ErrorFlag_ 2	[9]	Indicates whether the current value of BYTE_PER_PACKET register is valid or not. 0: no error, 1: error Updated after BytePerPacket value is written. If 0, transmission can be started.
			[10-31]	Reserved

5.7 DATA_DEPTH: 630h

This register allows the user to control the endianness of Y16 images.

Format:

Field	Bit	Description
Data_Depth	[0-7]	Effective data depth of current image data. If read value of Data_Depth is zero, shall ignore this field. Read: Effective data depth Write: Ignored
Little_Endian	[8]	Little endian mode for 16-bit pixel formats only Write/Read: 0: Big endian mode (default on initialization) 1: Little endian mode
	[9-31	Reserved

5.8 BAYER_MONO_CTRL: 1050h

This register enables raw Bayer output in non-Format 7 Y8/Y16 modes.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature. 0: Not Available, 1: Available
	[1-30]	Reserved.
Bayer_Mono_Ctrl	[31]	Value 0: Disable raw Bayer output in mono modes, 1: Enable raw Bayer output in mono modes

5.9 IMAGE_DATA_FORMAT: 1048h (IIDC 1.31)

This register allows the user to specify various image data format parameters.

Mirror_Image_Ctrl allows the user to toggle between normal and mirror (horizontally flipped) image modes.

Bayer_Mono_Ctrl allows the user to control whether non-Format 7 Y8 or Y16 monochrome modes on a color camera will output monochrome (greyscale) or raw Bayer data.

> **Note:** Selecting a half-width, half-height image size and monochrome pixel format, such as 800 x 600 Y8, using non-Format 7 modes provides a monochrome binned image. In some cases, enabling raw Bayer output in mono mode provides a raw Bayer region of interest of 800 x 600, centered within the larger pixel array. This affects the field of view.

Y16_Data_Format controls the endianness of Y16 images – either IIDC 1394 DCAM-compliant mode (default) or PGR-specific (Intel-compatible) mode – as described below.

IIDC 1394 DCAM Y16 Mode			PGR-specific Y16 Mode		
Description	Data Format		Description	Data Format	
Actual bit depth: Dependent on ADC Bit alignment: MSB Byte alignment: Big Endian	0-7	8-15	Actual bit depth: Dependent on ADC Bit alignment: MSB Byte alignment: Little Endian	0-7	8-15
	98765432	10xxxxxx		10xxxxxx	98765432

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
Reserved	[1-22]	Reserved
Mirror_Image_Ctrl	[23]	Control horizontally flipped image modes 0: Disable image flip 1: Enable image flip
Bayer_Mono_Ctrl	[24]	Control raw Bayer output in non-Format 7 mono modes 0: Disable 1: Enable

Field	Bit	Description
Reserved	[25-30]	Reserved
Y16_Data_Format	[24-31]	Value: 0: PGR-specific mode 1: DCAM-compliant mode (default)

6 Image Acquisition

6.1 TRIGGER_MODE: 830h

Control of the register is via the *ON_OFF* bit and the *Trigger_Mode* and *Parameter* fields.

Format

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the Value field, 1: Control with the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-5]	Reserved
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
Trigger_Polarity	[7]	Select trigger polarity (except for Software_Trigger) 0: Trigger active low, 1: Trigger active high
Trigger_Source	[8-10]	Select trigger source: used to select which GPIO pin will be used for external trigger purposes. Sets trigger source ID from *Trigger_Source_Inq* field of TRIGGER_INQ register(page 11).
Trigger_Value	[11]	Trigger input raw signal value: used to determine the current raw signal value on the pin. Read only 0: Low, 1: High
	[8-11]	Reserved
Trigger_Mode	[12-15]	Trigger mode (Trigger_Mode_0..15): used to set the trigger mode to be used. For more information, see Asynchronous Triggering. Query the *Trigger_Mode_Inq* fields of the TRIGGER_INQ register for available trigger modes.
	[16-19]	Reserved
Parameter	[20-31]	Parameter for trigger function, if required (optional)

6.2 TRIGGER_DELAY: 834h

Delay is in units of a 24.576 MHz clock. Less than 1024 ticks is linear; greater than 1024 ticks is non-linear. Consider using register 950h ABS_VAL_TRIGGER_DELAY .

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the Value field, 1: Control with the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-5]	Reserved
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
	[7-19]	Reserved
Value	[20-31]	Value.

6.3 PIO_DIRECTION: 11F8h

If the *IOx_Mode* bit is asserted (write a '1'), this means the GPIO pin is currently configured as an output and the *Pin_Mode* of the GPIO pin (see the GPIO_CTRL_PIN_x register) is GPIO_Mode_8. Otherwise, the *Pin_Mode* will be GPIO_Mode_0 (Input). The PIO_DIRECTION register is writeable only when the current GPIO_Mode is GPIO_Mode_0 or GPIO_Mode_8.

Format

Field	Bit	Description
IO0_Mode	[0]	Current mode of GPIO IO0 0: Input, 1: Output
IO1_Mode	[1]	Current mode of GPIO IO1 0: Input, 1: Output
IO2_Mode	[2]	Current mode of GPIO IO2 0: Input, 1: Output
IO3_Mode	[3]	Current mode of GPIO IO3 0: Input, 1: Output
	[4-31]	Reserved

6.4 SOFTWARE_TRIGGER: 62Ch

Note: Bit 0 of this register indicates if the camera is ready to be triggered again for both software and hardware triggering.

Format:

Field	Bit	Description
Software_Trigger	[0]	This bit automatically resets to zero in all trigger modes except Trigger Mode 3. Read: 0: Ready, 1: Busy Write: 0: Reset software trigger, 1: Set software trigger

6.5 ISO_CHANNEL/ISO_SPEED: 60Ch

Allows the user to query the camera's isochronous transmission channel and speed information.

Format:

Field	Bit	Description
ISO_Channel	[0-3]	Isochronous channel number for video data transmission (Except for Format_6)
	[4-5]	Reserved
ISO_Speed	[6-7]	Isochronous transmit speed code. (Except for Format_6) 0 = 100 Mbps 1 = 200 Mbps 2 = 400 Mbps
	[8-15]	Reserved
Operation_Mode	[16]	1394 operation mode Change control register sets of ISO_Channel and ISO_Speed registers 0 = Legacy (v1.30 compatible), 1 = 1394.b (v1.31 mode) Camera shall start in legacy mode for backward compatibility
	[17]	Reserved
ISO_Channel_B	[18-23]	Isochronous channel number for video data transmission of 1394.b mode (Except for Format_6)
	[24-28]	Reserved
ISO_Speed_B	[29-31]	Isochronous transmit speed code of 1394.b mode. (Except for Format_6) 0 = 100 Mbps 1 = 200 Mbps 2 = 400 Mbps 3 = 800 Mbps 4 = 1.6 Gbps 5 = 3.2 Gbpss

6.6 ISO_EN/CONTINUOUS_SHOT: 614h

This register allows the control of isochronous data transmission. During ISO_EN = 1 or One_Shot = 1 or Multi_Shot =1, the register value which reflects the Isochronous packet format cannot change. Data transfer control priority is ISO_EN > One_Shot > Multi_Shot.

Format:

Field	Bit	Description
ISO_EN/Continuous Shot	[0]	0 = Stop ISO transmission of video data. Continuous Shot is not enabled. 1 = Start ISO transmission of video data.
	[1-31]	Reserved.

6.7 ONE_SHOT/MULTI_SHOT: 61Ch

This register allows the user to control single and multi-shot functionality of the camera. During ISO_EN = 1, *One_Shot* = 1 or *Multi_Shot* =1, the register value which reflects the Isochronous packet format cannot change. Data transfer control priority is ISO_EN > One_Shot > Multi_Shot.

Single (One_Shot) transmission is used to transmit the last image without deleting it. Multi-shot transmission is used to transmit the *n* (Count_Number) oldest images and then deletes them.

Format:

Field	Bit	Description
One_Shot	[0]	1 = only one frame of video data is transmitted. (Self cleared after transmission) Ignored if ISO_EN = 1
Multi_Shot	[1]	1 = N frames of video data is transmitted. (Self cleared after transmission) Ignored if ISO_EN = 1 or One_Shot =1
	[2-15]	Reserved.
Count_Number	[16-31]	Count number for Multi-shot function.

6.8 Asynchronous Triggering

The camera supports asynchronous triggering, which allows the start of exposure (shutter) to be initiated by an external electrical source (or hardware trigger) or camera register write from an internal software mechanism (software trigger).

> **Note:** Not all camera models support all trigger modes. See your camera's Technical Reference for a list of supported modes.

6.8.1 Standard External Trigger (Mode 0)

Trigger Mode 0 is best described as the standard external trigger mode. When the camera is put into Trigger Mode 0, the camera starts integration of the incoming light from external trigger input falling/rising edge. The Shutter value describes integration time. No parameter is required. The camera can be triggered in this mode by using the GPIO pins as external trigger or by using a software trigger.

It is not possible to trigger the camera at full frame rate using Trigger Mode 0; however, this is possible using Overlapped Exposure Readout Trigger (Mode 14).

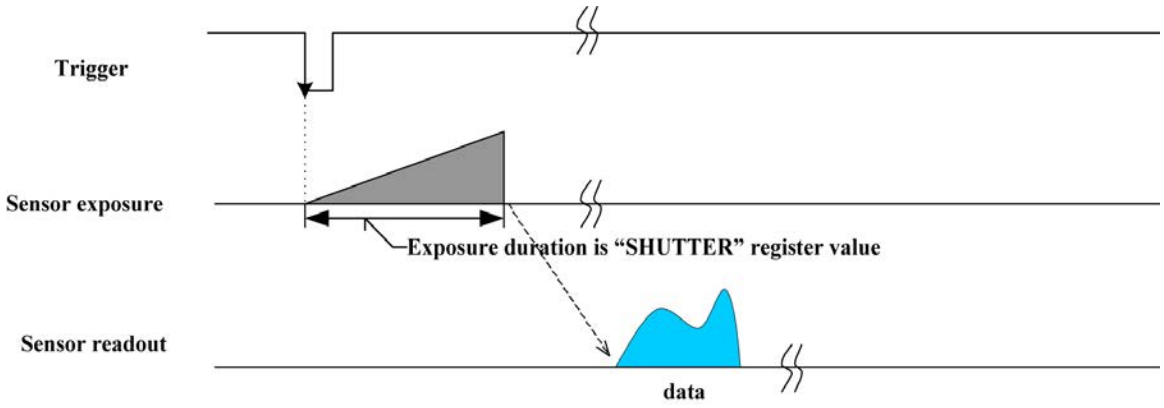


Figure 6.1: Trigger Mode 0 ("Standard External Trigger Mode")

Note: For FL3-U3-32S2 and FL3-U3-88S2 models operating in this trigger mode, exposure is controlled by the global reset feature of the sensor. This feature may reduce distortion artifacts typical of rolling shutter sensors.

Note: For the BFLY-PGE-50A2 models operating in this trigger mode, if the number of acquired images is 1, exposure is controlled by the global reset feature of the sensor. This feature may reduce distortion artifacts typical of rolling shutter sensors.

Registers—TRIGGER_MODE: 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_0
Parameter	[20-31]	None

6.8.2 Bulb Shutter Trigger (Mode 1)

Also known as Bulb Shutter mode, the camera starts integration of the incoming light from external trigger input. Integration time is equal to low state time of the external trigger input.

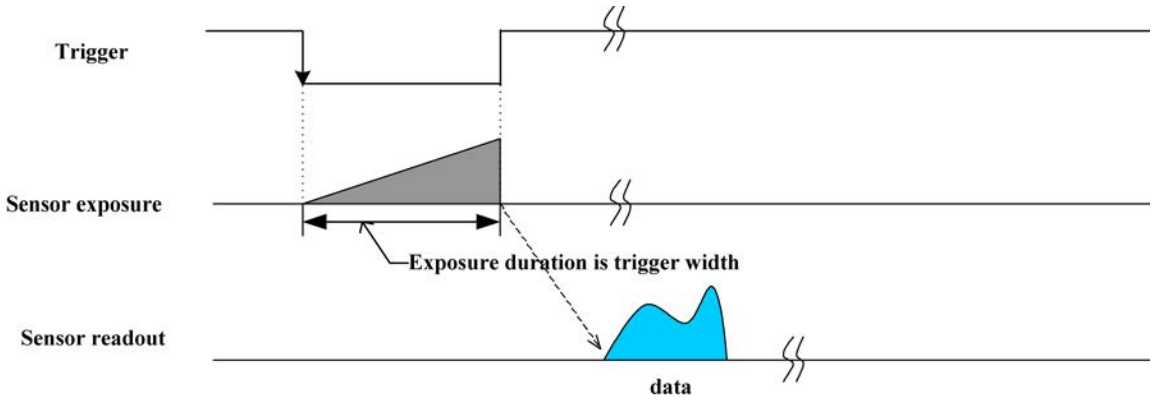


Figure 6.2: Trigger Mode 1 ("Bulb Shutter Mode")

Note: On FL3-U3-13Y3 a software trigger cannot be used for Trigger Mode 1.

Note: For FL3-U3-32S2 and FL3-U3-88S2 models operating in this trigger mode, exposure is controlled by the global reset feature of the sensor. This feature may reduce distortion artifacts typical of rolling shutter sensors.

Note: For the BFLY-PGE-50A2 models operating in this trigger mode, if the number of acquired images is 1, exposure is controlled by the global reset feature of the sensor. This feature may reduce distortion artifacts typical of rolling shutter sensors.

Registers—TRIGGER_MODE: 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_1
Parameter	[20-31]	None

6.8.3 Skip Frames Trigger (Mode 3)

Trigger Mode 3 allows the user to put the camera into a mode where the camera only transmits one out of N specified images. This is an internal trigger mode that requires no external interaction. Where N is the parameter set in the Trigger Mode, the camera will issue a trigger internally at a cycle time that is N times greater than the current frame rate. As with Trigger Mode 0, the Shutter value describes integration time. Note that this is different from the IIDC specification that states the cycle time will be N times greater than the fastest frame rate.

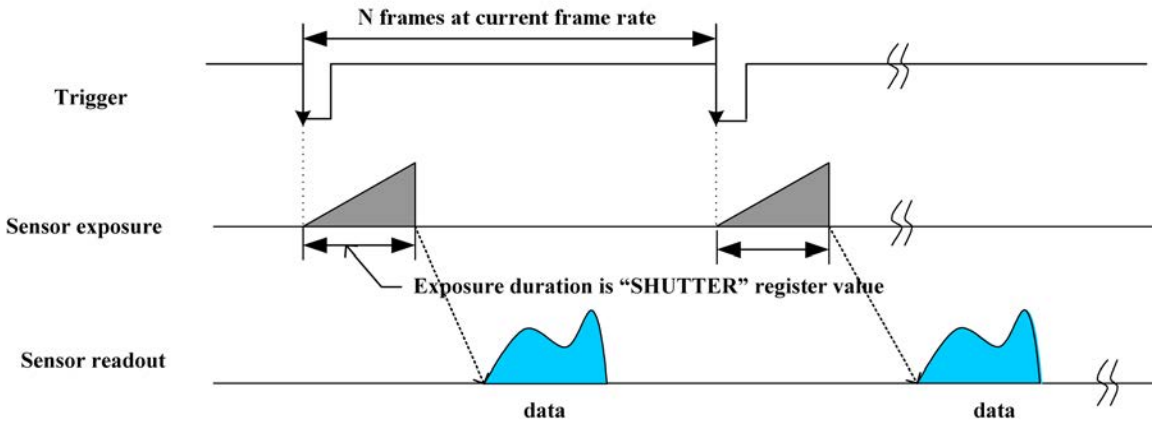


Figure 6.3: Trigger Mode 3 ("Skip Frames Mode")

Note: For FL3-GE, the debouncer does not work in trigger mode 3.

Registers—TRIGGER_MODE: 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_3
Parameter	[20-31]	*N* 1 out of N images is transmitted. Cycle time N times greater than current frame rate

6.8.4 Multiple Exposure Preset Trigger (Mode 4)

Trigger Mode 4 allows the user to set the number of triggered images to be exposed before the image readout starts. In the case of Trigger Mode 4, the shutter time is controlled by the Shutter value; the minimum resolution of the duration is therefore limited by the shutter resolution.

In the figure below, the camera starts integration of incoming light from the first external trigger input falling edge and exposes incoming light at shutter time. Repeat this sequence for N (parameter) external trigger inputs edge then finish integration. Parameter is required and shall be one or more (N >= 1).

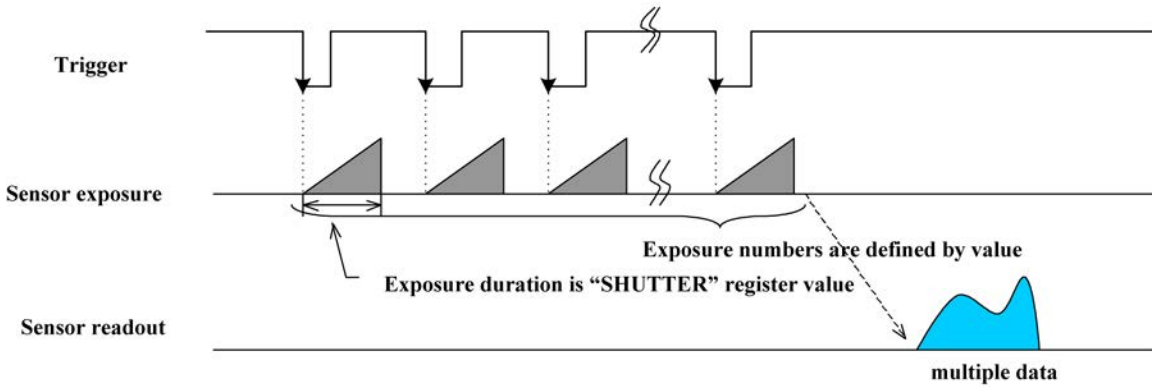


Figure 6.4: Trigger Mode 4 ("Multiple Exposure Preset Mode")

Registers—TRIGGER_MODE: 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_4
Parameter	[20-31]	N ≥ 1

6.8.5 Multiple Exposure Pulse Width Trigger (Mode 5)

Trigger Mode 5 allows the user to set the number of triggered images to be exposed before the image readout starts. In the case of Trigger Mode 5, the shutter time is controlled by the trigger pulse duration; the minimum resolution of the duration is generally 1 tick of the pixel clock (see PIXEL_CLOCK_FREQ: 1AF0h). The resolution also depends on the quality of the input trigger signal and the current trigger delay.

In the figure below, the camera starts integration of incoming light from the first external trigger input falling edge and exposes incoming light until the trigger is inactive. Repeat this sequence for N (parameter) external trigger inputs then finish integration. Parameter is required and shall be one or more (N ≥ 1).

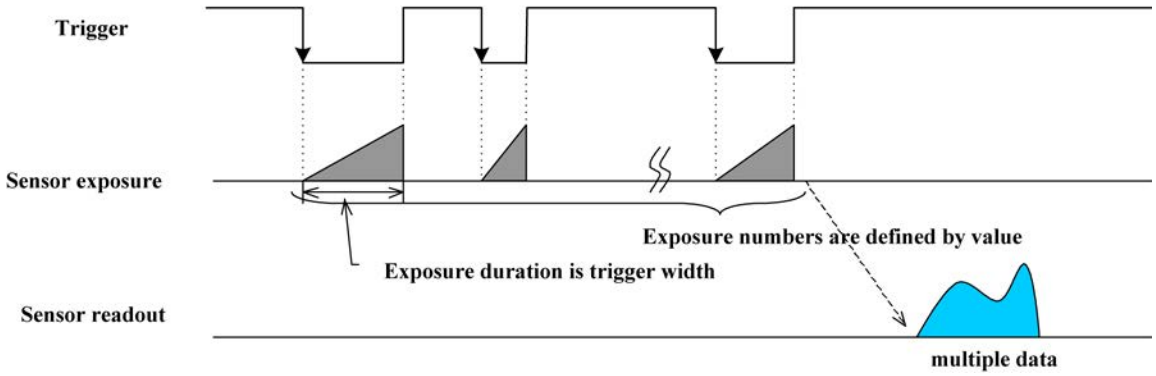


Figure 6.5: Trigger Mode 5 (“Multiple Exposure Pulse Width Mode”)

Registers—TRIGGER_MODE: 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_5
Parameter	[20-31]	N ≥ 1 number of images exposed before image readout starts

6.8.6 Low Smear Trigger (Mode 13)

Trigger Mode 13 is a reduced smear imaging mode.

Smear reduction works by increasing the speed of the vertical clock near the end of the integration cycle. This step is also known as fast dump. Since the clock speed has been increased, this reduces the time each pixel data has to collect smear while it passes through the vertical shift register.

This trigger mode behaves similarly to Standard External Trigger (Mode 0), except the trigger input first activates a fast dump off the CCD. The fast dump period is followed by exposure, which is controlled by the Shutter settings. The length of the fast dump period is determined by the trigger delay.

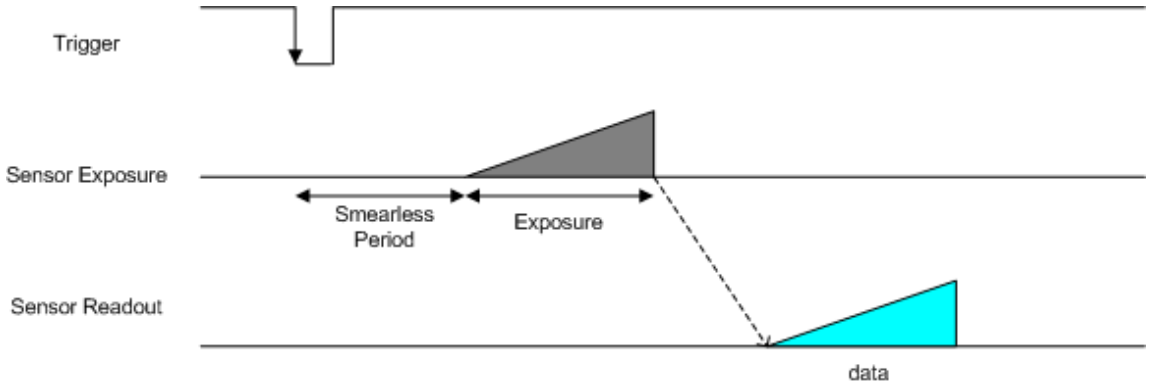


Figure 6.6: Trigger Mode 13 (“Low Smear Trigger Mode”)

Note: If specifying a trigger delay (see TRIGGER_DELAY: 834h) in this mode, the delay time must be specified as an absolute value (see Absolute Value Registers).

Registers—TRIGGER_MODE: 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_13
Parameter	[20-31]	None

6.8.7 Overlapped Exposure Readout Trigger (Mode 14)

Trigger Mode 14 is a vendor-unique trigger mode that is very similar to Trigger Mode 0, but allows for triggering at faster frame rates. This mode works well for users who want to drive exposure start with an external event. However, users who need a precise exposure start should use Trigger Mode 0.

In the figure below, the trigger may be overlapped with the readout of the image, similar to continuous shot (free-running) mode. If the trigger arrives after readout is complete, it will start as quickly as the imaging area can be cleared. If the trigger arrives before the end of shutter integration (that is, before the trigger is *armed*), it is dropped. If the trigger arrives while the image is still being read out of the sensor, the start of exposure will be delayed until the next opportunity to clear the imaging area without injecting noise into the output image. The end of exposure cannot occur before the end of the previous image readout. Therefore, exposure start may be delayed to ensure this, which means priority is given to maintaining the proper exposure time instead of to the trigger start.

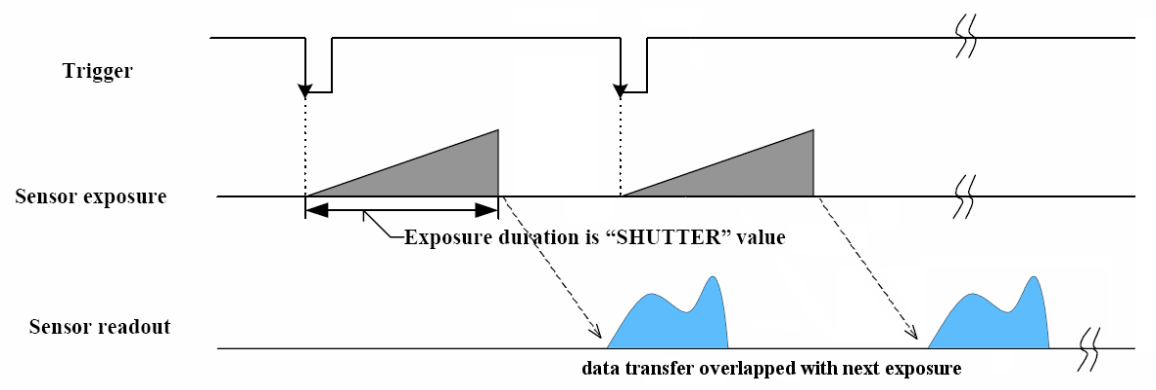


Figure 6.7: Trigger Mode 14 ("Overlapped Exposure/Readout Mode")

Registers—TRIGGER_MODE: 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_14
Parameter	[20-31]	None

6.8.8 Multi-Shot Trigger (Mode 15)

Trigger Mode 15 is a vendor-unique trigger mode that allows the user to fire a single hardware or software trigger and have the camera acquire and stream a predetermined number of images.

The number of images to be acquired is determined by the parameter specified with the trigger mode. This allows up to 255 images to be acquired from a single trigger. Setting the parameter to 0 results in a non-free running, non-overlap mode. If Trigger Mode 14 is supported on the camera, setting the parameter to 0 results in a non-free running, overlap mode.

Once the trigger is fired, the camera will acquire *N* images with an exposure time equal to the value defined by the shutter, and stream the images to the host system at the current frame rate. Once this is complete, the camera can be triggered again to repeat the sequence.

Any changes to the trigger control cause the current sequence to stop.

> **Note:** During the capture of *N* images, the camera is still in an asynchronous trigger mode (essentially Trigger Mode 14), rather than continuous (free-running) mode. The result of this is that the frame rate is turned OFF, and the camera put into extended shutter mode. Users should ensure that the maximum shutter time is limited to 1/frame_rate to get the *N* images captured at the current frame rate.

Related Knowledge Base Articles

Title	Article
Extended shutter mode operation for DCAM-compliant FLIR machine vision products	Knowledge Base Article 10087

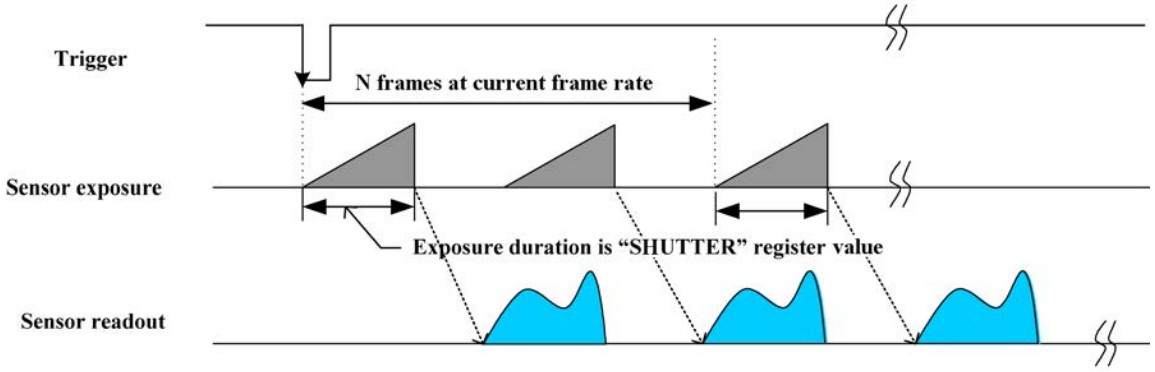


Figure 6.8: Trigger Mode 15 ("Multi-Shot Trigger Mode")

Note: For FL3-U3-32S2 and FL3-U3-88S2 models operating in this trigger mode, exposure is controlled by the global reset feature of the sensor. This feature may reduce distortion artifacts typical of rolling shutter sensors.

Note: For the BFLY-PGE-50A2 models operating in this trigger mode, if the number of acquired images is 1, exposure is controlled by the global reset feature of the sensor. This feature may reduce distortion artifacts typical of rolling shutter sensors.

Registers—TRIGGER_MODE: 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_15
Parameter	[20-31]	*N* number of images to be acquired

7 Camera Attributes

7.1 Imaging Parameters: 800h-888h

The following imaging parameters share the same register format.

Parameter	Register
Brightness	800h
Sharpness	808h
Hue	810h
Saturation	814h
Gamma	818h
Gain	820h
Iris	824h
Focus	828h
Pan	884h
Tilt	888h

These imaging parameters are defined by **modes** and **values**.

There are three modes:

Mode	Description
On/Off	Determines if the feature is on. If off, values are fixed and not controllable.
Auto/Manual	If the feature is on, determines if the feature is in automatic or manual mode. If manual, values can be set.
One Push	If the feature is in manual mode, the camera executes once automatically and then returns to manual mode.

The value field in this register can be set in three ways:

Method	Description
Absolute	The user sets the value is set via the absolute register. The *Value* field becomes read only and reflects the converted absolute value.
Manual	The user sets the value in the *Value* field. The absolute register becomes read only and contains the current value.
Automatic	The value is set automatically by another register and both the *Value* field and the absolute register become read only.

Note: Formulas for converting the fixed point (relative) values to floating point (absolute) values are not provided. Users wishing to work with real-world values should refer to Absolute Value CSRs.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Abs_Control	[1]	Absolute value control 0: Control in the Value field, 1: Control in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically only once) Read: 0: Not in operation, 1: In operation Write: 1: Begin to work (self-cleared after operation) If A_M_Mode = 1, this bit is ignored
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: read a current mode Write: set the mode 0: Manual, 1: Automatic
	[8-19]	Reserved
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.

7.2 Parameter Limits

Some imaging parameters may have their ranges limited by default to ensure best possible image quality. This limit can be removed to allow access to the full range.

Parameters that can be limited include:

- Gain

7.2.1 ParameterSelector: 5420h

Format:

Field	Bit	Description
Select_Parameter	[0-31]	0x00 = Gain

7.2.2 RemoveLimits: 5424h

Format:

Field	Bit	Description
	[0-30]	Reserved
Enable_RemoveLimits	[31]	Remove limits on the parameter selected in 5420h 0: Disabled, 1: Enabled Default is 0

7.3 LUT: 80000h – 80048h

Offset	Name	Field	Bit	Description
80000h	LUT_Ctrl_Inq (Read Only)	Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
			[1-4]	Reserved
		ON_OFF_Inq	[5]	Capability of turning this feature ON or OFF.
			[6-7]	Reserved
		Input_Depth	[8-12]	Input data bit depth
		Output_Depth	[13-17]	Output data bit depth
			[18]	Reserved
		Number_of_Channels	[19-23]	Number of channels
			[24-26]	Reserved
		Number_of_Banks	[27-31]	Number of banks

Offset	Name	Field	Bit	Description
80004h	LUT_Bank_Rd_Inq	Read_Bank_0_Inq	[0]	Capability of reading data from Bank 0
		Read_Bank_1_Inq	[1]	Capability of reading data from Bank 1
		Read_Bank_2_Inq	[2]	Capability of reading data from Bank 2
		Read_Bank_3_Inq	[3]	Capability of reading data from Bank 3
		Read_Bank_4_Inq	[4]	Capability of reading data from Bank 4
		Read_Bank_5_Inq	[5]	Capability of reading data from Bank 5
		Read_Bank_6_Inq	[6]	Capability of reading data from Bank 6
		Read_Bank_7_Inq	[7]	Capability of reading data from Bank 7
		Read_Bank_8_Inq	[8]	Capability of reading data from Bank 8
		Read_Bank_9_Inq	[9]	Capability of reading data from Bank 9
		Read_Bank_10_Inq	[10]	Capability of reading data from Bank 10
		Read_Bank_11_Inq	[11]	Capability of reading data from Bank 11
		Read_Bank_12_Inq	[12]	Capability of reading data from Bank 12
		Read_Bank_13_Inq	[13]	Capability of reading data from Bank 13
		Read_Bank_14_Inq	[14]	Capability of reading data from Bank 14
		Read_Bank_15_Inq	[15]	Capability of reading data from Bank 15
	LUT_Bank_Wr_Inq	Write_Bank_0_Inq	[16]	Capability of writing data to Bank 0
		Write_Bank_1_Inq	[17]	Capability of writing data to Bank 1
		Write_Bank_2_Inq	[18]	Capability of writing data to Bank 2
		Write_Bank_3_Inq	[19]	Capability of writing data to Bank 3
		Write_Bank_4_Inq	[20]	Capability of writing data to Bank 4
		Write_Bank_5_Inq	[21]	Capability of writing data to Bank 5
		Write_Bank_6_Inq	[22]	Capability of writing data to Bank 6
		Write_Bank_7_Inq	[23]	Capability of writing data to Bank 7
		Write_Bank_8_Inq	[24]	Capability of writing data to Bank 8
		Write_Bank_9_Inq	[25]	Capability of writing data to Bank 9
		Write_Bank_10_Inq	[26]	Capability of writing data to Bank 10
		Write_Bank_11_Inq	[27]	Capability of writing data to Bank 11
		Write_Bank_12_Inq	[28]	Capability of writing data to Bank 12
		Write_Bank_13_Inq	[29]	Capability of writing data to Bank 13
		Write_Bank_14_Inq	[30]	Capability of writing data to Bank 14
		Write_Bank_15_Inq	[31]	Capability of writing data to Bank 15

Offset	Name	Field	Bit	Description
80008h	LUT_Ctrl	Presence_Inq	[0]	Presence of this Feature 0: Not Available, 1: Available
			[1-4]	Reserved
		ON_OFF	[5]	Read: read a status Write: ON or OFF this feature 0: OFF 1: ON When ON is written, the ON_OFF field of the GAMMA register is turned to OFF.
			[6-27]	Reserved
		Active_Bank	[28-31]	Active bank
8000Ch	Bank_0_ Offset_Inq	Bank_0_Quadlet_Offset	[0-31]	32-bit offset of Bank 0 table data
80010h	Bank_1_ Offset_Inq	Bank_1_Quadlet_Offset	[0-31]	32-bit offset of Bank 1 table data
80014h	Bank_2_ Offset_Inq	Bank_2_Quadlet_Offset	[0-31]	32-bit offset of Bank 2 table data
80018h	Bank_3_ Offset_Inq	Bank_3_Quadlet_Offset	[0-31]	32-bit offset of Bank 3 table data
8001Ch	Bank_4_ Offset_Inq	Bank_4_Quadlet_Offset	[0-31]	32-bit offset of Bank 4 table data
80020h	Bank_5_ Offset_Inq	Bank_5_Quadlet_Offset	[0-31]	32-bit offset of Bank 5 table data
80024h	Bank_6_ Offset_Inq	Bank_6_Quadlet_Offset	[0-31]	32-bit offset of Bank 6 table data
80028h	Bank_7_ Offset_Inq	Bank_7_Quadlet_Offset	[0-31]	32-bit offset of Bank 7 table data
8002Ch	Bank_8_ Offset_Inq	Bank_8_Quadlet_Offset	[0-31]	32-bit offset of Bank 8 table data
80030h	Bank_9_ Offset_Inq	Bank_9_Quadlet_Offset	[0-31]	32-bit offset of Bank 9 table data
80034h	Bank_10_ Offset_Inq	Bank_10_Quadlet_Offset	[0-31]	32-bit offset of Bank 10 table data
80038h	Bank_11_ Offset_Inq	Bank_11_Quadlet_Offset	[0-31]	32-bit offset of Bank 11 table data
8003Ch	Bank_12_ Offset_Inq	Bank_12_Quadlet_Offset	[0-31]	32-bit offset of Bank 12 table data
80040h	Bank_13_ Offset_Inq	Bank_13_Quadlet_Offset	[0-31]	32-bit offset of Bank 13 table data
80044h	Bank_14_ Offset_Inq	Bank_14_Quadlet_Offset	[0-31]	32-bit offset of Bank 14 table data
80048h	Bank_15_ Offset_Inq	Bank_15_Quadlet_Offset	[0-31]	32-bit offset of Bank 15 table data

7.4 LUT: 1A40h – 1A44h (IIDC 1.31)

Note: Cameras using the IIDC Specification version 1.31 must use the following lookup table registers.

This register allows the user to access and control a lookup table (LUT), with entries stored onboard the camera. Changes to GAMMA are translated to writes of the LUT CSR registers. The LUT will also be modifed under the following circumstances:

- Camera reinitialization via the INITIALIZE register 000h
- Changing the CURRENT_VIDEO_MODE or CURRENT_VIDEO_FORMAT registers 604h or 608h
- Changing the GAMMA register 818h or ABS_VAL_GAMMA register
- Changing the WHITE_BALANCE register 80Ch (SCOR-13FF only)
- Writing the AUTO_EXPOSURE_RANGE register 108Ch (Flea only)

Offset	Name	Field	Bit	Description
1A40h	LUT_LO_ CTRL	Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
			[1-2]	Reserved
		Num_Channels	[3-5]	Number of channels
		ON_OFF	[6]	Write: ON or OFF for this feature Read: Read a status 0: OFF, 1: ON If this bit = 0, other fields are read only
			[7]	Reserved
		Bit_Depth	[8-15]	Bit depth of the lookup table
		Entries	[16-31]	Number of entries in the table
1A44h	LUT_HI_INQ		[0-31]	32-bit offset of the lookup table

7.5 WHITE_BALANCE: 80Ch

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the Value field, 1: Control with the Absolute Value CSR If this bit is 1, then Value is ignored
	[2-4]	Reserved

Field	Bit	Description
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Read: 0: Not in operation, 1: In operation Write: 1: Begin to work (self-cleared after operation) If A_M_Mode = 1, this bit is ignored
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: read the current mode. Write: Set the mode. 0: Manual, 1: Auto
U_Value/B_Value	[8-19]	Blue Value. A write to this value in 'Auto' mode will be ignored.
V_Value/R_Value	[20-31]	Red Value. A write to this value in 'Auto' mode will be ignored.

7.6 BAYER_TILE_MAPPING: 1040h

This 32-bit read only register specifies the sense of the cameras' Bayer tiling. Various colors are indicated by the ASCII representation of the first letter of their name.

Color	ASCII
Red (R)	52h
Green (G)	47h
Blue (B)	42h
Monochrome (Y)	59h

For example, 0x52474742 is RGGB and 0x59595959 is YYYY.

Note: Because color models support on-board color processing, the camera reports YYYY tiling when operating in any non-raw Bayer data format.

Format

Field	Bit	Description
Bayer_Sense_A	[0-7]	ASCII representation of the first letter of the color of pixel (0,0) in the Bayer tile.
Bayer_Sense_B	[8-15]	ASCII representation of the first letter of the color of pixel (0,1) in the Bayer tile.
Bayer_Sense _C	[16-24]	ASCII representation of the first letter of the color of pixel (1,0) in the Bayer tile.
Bayer_Sense _D	[25-31]	ASCII representation of the first letter of the color of pixel (1,1) in the Bayer tile.

7.7 MIRROR_IMAGE_CTRL: 1054h

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature. 0: Not Available, 1: Available
	[1-30]	Reserved.
Mirror_Image_Ctrl	[31]	Value 0: Disable horizontal (mirror) image flip 1: Enable horizontal (mirror) image flip

7.8 SHUTTER: 81Ch

This register has three states:

State	Description
Manual/Abs	The shutter value is set by the user via the ABS_VAL_SHUTTER register . The *Value* field becomes read only and reflects the converted value of the ABS_VAL_SHUTTER register.
Manual	The user sets the shutter value via the *Value* field. The ABS_VAL_SHUTTER register becomes read only and contains the current shutter time.
Auto	The shutter value is set by the auto exposure controller (if enabled) . Both the *Value* field and the ABS__VAL_SHUTTER register become read only.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the *Value* field, 1: Control with the Absolute value CSR. If this bit = 1, the value in the *Value* field is ignored.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Read: 0: Not in operation, 1: In operation Write: 1: Begin to work (self-cleared after operation) If A_M_Mode = 1, this bit is ignored
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: read a current mode Write: set the mode 0: Manual, 1: Automatic
High_Value	[8-19]	Upper 4 bits of the shutter value available only in extended shutter mode (outside of specification).

Field	Bit	Description
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.

7.9 AUTO_EXPOSURE: 804h

Note: Formulas for converting the fixed point (relative) values to floating point (absolute) values are not provided. Users wishing to work with real-world values should refer to Absolute Value CSRs.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the *Value* field, 1: Control with the Absolute value CSR. If this bit = 1, the value in the *Value* field is ignored.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Read: 0: Not in operation, 1: In operation Write: 1: Begin to work (self-cleared after operation) If A_M_Mode = 1, this bit is ignored
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: read a current mode Write: set the mode 0: Manual, 1: Automatic
High_Value	[8-19]	Upper 4 bits of the shutter value available only in extended shutter mode (outside of specification).
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.

7.9.1 AUTO_EXPOSURE_RANGE: 1088h

Fixed point (relative) values must be specified. Do not specify absolute values.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-7]	Reserved
Min_Value	[8-19]	Lower bound
Max_Value	[20-31]	Upper bound

7.9.2 AUTO_SHUTTER_RANGE: 1098h

Fixed point (relative) values must be specified. Do not specify absolute values.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
Min_Dark_Noise	[6]	Minimizes dark current noise with extended shutter times. This feature is currently experimental. 0: Disable dark noise minimization, 1: Enable dark noise minimization
	[7]	Reserved
Min_Value	[8-19]	Lower bound
Max_Value	[20-31]	Upper bound

Note: The actual range used is further restricted to match the current grab mode (see SHUTTER: 81Ch for the list of ranges).

7.9.3 AUTO_GAIN_RANGE: 10A0h

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
	[7]	Reserved
Min_Value	[8-19]	Lower bound
Max_Value	[20-31]	Upper bound

7.9.4 AE_ROI: 1A70 – 1A74h

AE_ROI is not supported on quad tap sensor cameras.

> **Note:** To calculate the base address for an offset CSR:
> 1. Query the offset inquiry register.
> 2. Multiple the value by 4. (The value is a 32-bit offset.)
> 3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

Format:

Offset	Name	Field	Bit	Description
1A70h	AE_ROI_CTRL	Presence_Inq	[0]	Presence of this feature 0:Not Available, 1: Available
			[1-5]	Reserved
		ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
			[7-31]	Reserved
1A74h	AE_ROI_OFFSET		[0-31]	32-bit offset for the AE_ROI CSRs
Base + 0h	AE_ROI_UNIT_POSITION_INQ	Hposunit	[0-15]	Horizontal units for position
		Vposunit	[16-31]	Vertical units for position
Base + 4h	AE_ROI_UNIT_SIZE_INQ	Hunit	[0-15]	Horizontal units for size
		Vunit	[16-31]	Vertical units for size
Base + 8h	AE_ROI_POSITION	Left	[0-15]	Left position of ROI
		Top	[16-31]	Top position of ROI
Base + Ch	AE_ROI_SIZE	Width	[0-15]	Width of ROI
		Height	[16-31]	Height of ROI

7.10 HDR: 1800h – 1884h

This register allows the user to access and control a multiple exposure quick cycle mode, which is useful for high dynamic range (HDR) imaging.

Note that if bit [31] of the FRAME_INFO: 12F8h is set to 1, the camera will embed the current shutter/gain value in the image when bit [6] of HDR_CTRL is set to 1. The image timestamp will be embedded in the first 32-bits of image data, the shutter value in the second 32-bits, and gain in the third, all in big-endian format.

Note that the on/off bit for the HDR shutter and gain registers is hard-coded to on.

Format:

Offset	Name	Field	Bit	Description
1800h	HDR_CTRL	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-5]	Reserved
		ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
		-	[7-31]	Reserved
1820h	HDR_SHUTTER_0	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-19]	Reserved
		Value	[20-31]	Query SHUTTER_INQ register 51Ch for range of possible shutter values
1824h	HDR_GAIN_0	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-19]	Reserved
		Value	[20-31]	Query GAIN_INQ register 520h for range of possible gain values
1840h	HDR_SHUTTER_1	Same format as HDR_SHUTTER_0		
1844h	HDR_GAIN_1	Same format as HDR_GAIN_0		
1860h	HDR_SHUTTER_2	Same format as HDR_SHUTTER_0		
1864h	HDR_GAIN_2	Same format as HDR_GAIN_0		
1880h	HDR_SHUTTER_3	Same format as HDR_SHUTTER_0		
1884h	HDR_GAIN_3	Same format as HDR_GAIN_0		

7.11 NOISE_REDUCTION: 1224h

Allows control of the camera's noise filter mechanism.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-6]	Reserved

Field	Bit	Description
A_M_Mode	[7]	Read: read a current mode Write: set the mode 0: Manual, 1: Automatic In manual mode, the filter mechanism is controlled by the Filter field. In automatic mode: If camera gain < lower gain threshold, no filter is applied If lower gain threshold <= camera gain > upper gain threshold, median filter is applied If camera gain >= upper gain threshold, linear filter is applied. Lower gain threshold and upper gain threshold are defined by GAIN_THRESHOLD register 1228h (page 74).
	[8-29]	Reserved
Filter	[30-31]	Value: 0: no filter 1: median filter 2: linear filter

7.12 GAIN_THRESHOLD: 1228h

Specifies the lower and upper gain thresholds for operating the camera's noise reduction mechanism in auto mode, as controlled by the A_M_Mode field of register (page 73).

Format:

Field	Bit	Description
	[0-7]	Reserved
Upper_Gain_Threshold	[8-19]	Upper gain threshold. Default value is 1CEh, or approximately 14 dB.
Lower_Gain_Threshold	[20-31]	Lower gain threshold. Default value is 295h, or approximately 21 dB.

7.13 HDSDI CTRL

Format:

Address	Name	Field	Bit	Description
1B00h	Inquiry Register			
1B04h	Output Resolution	Outputs the current resolution of the HD image; 1920 x 1080, 1280 x 720, or 1600 x 1200	[0-15]	Width
			[16-31]	Height

Address	Name	Field	Bit	Description
1B08h	Control Register	Cutout or Stretch Mode	[0-7]	0x82 = manual cutout mode 0x83 = auto cutout mode 0xC2 = manual stretch mode 0xC3 = auto stretch mode 0xE3 = stamp mode
			[8-29]	Reserved
		HD Format Manual mode/Auto stretch mode: All three options available. Auto cut out mode: Only 0 and 1 available; camera chooses based on image size.	[30-31]	0: 1080p, 1: 720p, 2: 1200p
1B10h	Offset Unit Position Register		[0-15]	Offset multiple of x
			[16-31]	Offset multiple of y
1B14h	Offset Register		[0-15]	Offset in the x
			[16-31]	Offset in the y
1B18h	Offset Zoom Register		[0-15]	Offset in the x
			[16-31]	Offset in the y
1B1Ch	Offset Resolution Register		[0-15]	Width of zoom
			[16-31]	Height of zoom
1B20h	Embedded Data		[31]	0: disabled, 1: embedded serial data

7.14 IRIS: 824h

Note: Always attach the lens before setting any parameters.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: read a current mode Write: set the mode 0: Manual, 1: Automatic

Field	Bit	Description
	[8-19]	Reserved
Value	[20-31]	Value If in Manual mode, can fully closed (0; 00h) or fully open (255; FFh) If in Auto mode, a write to this value will be ignored.

7.15 P_IRIS: 1B24h

Note: Always disable P-Iris before installing a new lens or changing parameters. It is the enabling of P-Iris that initiates lens calibration.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: read a current mode Write: set the mode 0: Manual, 1: Automatic
	[8-23]	Reserved
Maximum_Range	[24-31]	Maximum allowed range for the P-Iris (dependent on lens) If in Auto mode, this value must be defined

7.16 P_IRIS: 1B28h

Note: Always disable P-Iris before installing a new lens or changing parameters. It is the enabling of P-Iris that initiates lens calibration.

Format:

Field	Bit	Description
Step_Period	[0-19]	P-Iris µs per step Defaults to 5000 µs. May need to be adjusted per lens manufacturer's specifications.
Current_Position	[20-31]	The Current Position of the iris. If in Manual mode (1B24h), this value can be set according to lens manufacturer's specifications. If in Auto mode (1B24h), this value is read only.

7.17 JPEG_CTRL: 1E80h

Specifies the JPEG compression rate.

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
RTP_ON_OFF	[1]	Enable/disable RTP transmission 0: RTP is OFF, 1: RTP is ON
	[2-5]	Reserved
ON_OFF	[6]	JPEG compression ON_OFF. Read: Read the current status Write: Set the status 0: JPEG compression is OFF, 1: JPEG compression is ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: Read a current mode Write: Set the mode 0: Manual, 1: Automatic JPEG quality control
	[8-23]	Reserved
Value	[24-31]	JPEG quality value. Valid range: 0x01 (1%) to 0x64 (100%). A value of 0 is treated as 60%. A write to this value in 'Auto' mode will be ignored.

7.18 JPEG_BUFFER_USAGE: 1E84h

This register is for Ladybug cameras only.

Specifies the percentage of the image buffer on the PC that is used for JPEG compressed image data, when the camera is operating in a JPEG mode.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-24]	Reserved

Field	Bit	Description
Value	[25-31]	Value. Valid range: 0x00 (0%) to 0x7F (100%) A value of 0 is treated as 0x66 (80%). On Ladybug3 firmware v1.2.2.1 or later, a value of 0 is treated as 0x72 (90%).

7.19 JPEG_PACKET: 1E88h

Specifies the JPEG packet delay used for RTP/UDP transmission. This is distinct from and does not affect the GigEPacket Delay.

Field	Bit	Description
Packet_Delay	[0-31]	Packet delay used by RTSP in multiples of 32. 1 = 32 ticks Default value is 3907 (i.e., 125024/32)

7.20 Embedded Image Information

This setting controls the frame-specific information that is embedded into the first several pixels of the image. The first byte of embedded image data starts at pixel 0,0 (column 0, row 0) and continues in the first row of the image data: (1,0), (2,0), and so forth. Users using color cameras that perform Bayer color processing on the computer must extract the value from the non-color processed image in order for the data to be valid.

Note: Embedded image values are those in effect at the end of shutter integration.

Each piece of information takes up 32-bits (4 bytes) of the image. When the camera is using an 8- bit pixel format , this is 4 pixels worth of data.

The following frame-specific information can be provided:

- Timestamp
- Gain
- Shutter
- Brightness
- White Balance
- Frame counter
- Strobe Pattern counter
- GPIO pin state
- ROI position

If you turned on all possible options the first 40 bytes of image data would contain camera information in the following format, when accessed using the FlyCapture 2 API:

(assuming `unsigned char* data = rawImage.GetData();` and an `Image` object `rawImage`):

- data[0] = first byte of Timestamp data
- data[4] = first byte of Gain data
- data[24] = first byte of Frame Counter data

If only Shutter embedding were enabled, then the first 4 bytes of the image would contain Shutter information for that image. Similarly, if only Brightness embedding were enabled, the first 4 bytes would contain Brightness information.

For monochrome cameras, white balance is still included, but no valid data is provided.

To access embedded information:

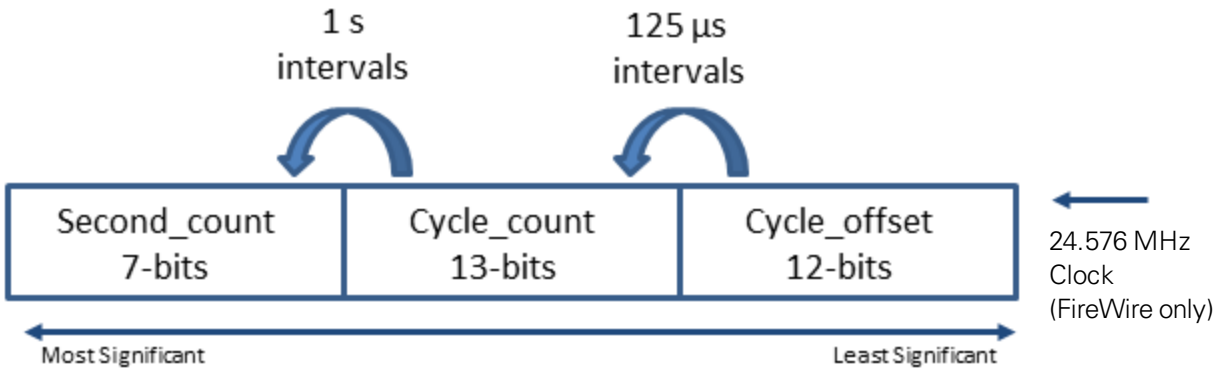
- CSRs—FRAME_INFO: 12F8h

Interpreting Timestamp information

The CYCLE_TIME register is located at 1EA8h.

The CYCLE_TIME register is located at 0xFF100200.

The Timestamp format is as follows (some cameras replace the bottom 4 bits of the cycle offset with a 4-bit version of the Frame Counter):



FireWire: Cycle_offset increments from 0 to 3071, which equals one cycle_count.

GigE, USB2, USB3: Cycle_offset increments from 0 to *x* depending on implementation, where *x* equals one cycle_count.

Cycle_count increments from 0 to 7999, which equals one second.

Second_count increments from 0 to 127.

All counters reset to 0 at the end of each cycle.

> **Note:** On USB and GigE devices, the four least significant bits of the timestamp do not accurately reflect the cycle_offset and should be discounted.

Interpreting ROI information

The first two bytes are the distance from the left frame border that the region of interest (ROI) is shifted. The next two bytes are the distance from the top frame border that the ROI is shifted.

7.20.1 FRAME_INFO: 12F8h

Field	Bit	Description	Frame-Specific Information
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
	[1-5]	Reserved	
ROI_Pos_Inq	[6]	Presence of image-specific information display 0: Not Available, 1: Available	
GPIO_State_Inq	[7]		
Strobe_Pat_Inq	[8]		
Frame_Count_Inq	[9]		
WB_CSR_Inq	[10]		
Exp_CSR_Inq	[11]		
Bright_CSR_Inq	[12]		
Shutter_CSR_Inq	[13]		
Gain_CSR_Inq	[14]		
Time_Inq	[15]		
CSR_Abs_Value	[16]	Toggles between displaying 32-bit relative or absolute CSR values. If absolute value not supported, relative value is displayed. 0: Relative, 1: Absolute This field is currently read-only	
	[17-21]	Reserved	
Insert_Info	[22]	Display image-specific information 0: Off 1: On	Region of Interest (ROI) position (See page 79)
	[23]		GPIO Pin State
	[24]		Strobe Pattern Counter
	[25]		Frame Counter
	[26]		White Balance CSR
	[27]		Exposure CSR
	[28]		Brightness CSR
	[29]		Shutter Value
	[30]		Gain CSR
	[31]		Timestamp (See page 79)

8 Troubleshooting

8.1 Downloads and Support

FLIR endeavors to provide the highest level of technical support possible to our customers. Most support resources can be accessed through the Support section of our website.

The first step in accessing our technical support resources is to obtain a Customer Login Account. This requires a valid name and email address. To apply for a Customer Login Account go to our Downloads page.

Customers with a Customer Login Account can access the latest **software** and **firmware** for their cameras from our website. We encourage our customers to keep their software and firmware up-to-date by downloading and installing the latest versions.

8.1.1 Finding Information

FlyCapture SDK—The FlyCapture SDK provides API examples and the FlyCap camera evaluation application. Available from our Downloads page.

API Documentation—The installation of the FlyCapture SDK comes with API references for C++, C#, and C code. Available from Start Menu→All Programs→Point Grey FlyCapture2 SDK→Documentation

Product Documentation—The camera's *Getting Started Manual* provides information on installing components and software needed to run the camera. The *Technical Reference* provides information on the camera's specifications, features and operations, as well as imaging and acquisition controls. They are available from the Downloads page.

Knowledge Base—A database of articles and application notes with answers to common questions as well as articles and tutorials about hardware and software systems. Available from our Knowledge Base.

Learning Center—Our Learning Center contains links to many resources including videos, case studies, popular topics, other application notes, and information on sensor technology.

8.1.2 Contacting Technical Support

Before contacting Technical Support, have you:

1. Read the product documentation?
2. Searched the Knowledge Base?
3. Downloaded and installed the latest version of software and/or firmware?

If you have done all the above and still can't find an answer to your question, contact our Technical Support team.

8.2 Camera Diagnostics

Use the following parameters to monitor the error status of the camera and troubleshoot problems:

Initialize—This allows the user to reset the camera to its initial state and default settings.

Time from Initialize—This reports the time, in seconds, since the camera was initialized during a hard power-up. This is different from powering up the camera, which will not reset this time.

Time from Bus Reset—This reports the time, in seconds, since the last bus reset occurred. This will be equal to the Time from Initialize if no reset has occurred since the last time the camera was initialized.

Link Up Time—This reports the time, in seconds, since the last Ethernet reconnection occurred. This will be equal to the Time from Initialize if no reconnection has occurred since the last time the camera was initialized.

Transmit Failure—This contains a count of the number of failed frame transmissions that have occurred since the last reset. An error occurs if the camera cannot arbitrate for the bus to transmit image data and the image data FIFO overflows.

Video Mode Error—This reports any camera configuration errors. If an error has occurred, no image data will be sent by the camera.

Camera Log—This provides access to the camera's 256 byte internal message log, which is often useful for debugging camera problems. Contact technical support for interpretation of message logs.

8.2.1 INITIALIZE: 000h

Format:

Offset	Name	Field	Bit	Description
000h	INITIALIZE	Initialize	[0]	If this bit is set to 1, the camera will reset to its power up state and loads settings from the last save memory channel. This bit is self-cleared.
			[1-31]	Reserved

8.2.2 TIME_FROM_INITIALIZE: 12E0h

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Time_From_Init	[1-31]	Time in seconds since the camera was initialized.

8.2.3 TIME_FROM_BUS_RESET / LINK_UP_TIME: 12E4h

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Time_From_Reset	[1-31]	Time in seconds since the camera detected a bus reset re-connection.

8.2.4 XMIT_FAILURE: 12FCh

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Frame_Count	[1-31]	Read: Count of failed frame transmissions. Write: Reset.

8.2.5 VMODE_ERROR_STATUS: 628h

Format:

Field	Bit	Description
Vmode_Error_Status	[0]	Error status of combination of video format, mode, frame rate and ISO_SPEED setting. 0: no error, 1: error This flag will be updated every time one of the above settings is changed by writing a new value.
	[1-31]	Reserved.

8.2.6 TEST_PATTERN: 104Ch

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-30]	Reserved
Test_Pattern_1	[31]	Value 0: Disable test pattern, 1: Enable test pattern

8.2.7 LED_CTRL: 1A14h

Note: On GigE Vision cameras, this register enables or disables both the main camera status LED and the GigE connector indicator LEDs, if equipped.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-22]	Reserved
LED_Ctrl	[23-31]	Enable or disable the LED 0x00: Off, 0x74: On

8.3 PIXEL_DEFECT_CTRL: 1A60h

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
	[5]	**FL3-U3-13E4 only**—Enable or disable on-sensor pixel correction 0: Off, 1: On
ON_OFF	[6]	Enable or disable FPGA pixel correction 0: Off, 1: On
	[7]	Reserved
Max_Pixels	[8-19]	Maximum number of pixels that can be corrected by the FPGA
Cur_Pixels	[20-31]	Current number of pixels that are being corrected by the FPGA
FL3-U3-13E4 only—If both bits 5 and 6 are set to 1, only the on-sensor pixel correction is enabled.		

8.4 FPN_CTRL: 1A0Ch

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Enable or disable fixed pattern noise correction 0: Off, 1: On
Reserved	[7-31]	Reserved

Appendix A: Isochronous Packet Format

The information in this appendix is applicable to FireWire cameras only.

The following table shows the format of the first 32-bits in the data field of an isochronous data block for Format 0, Format 1, Format 2, and Format 7.

Table A.1: Isochronous Data Packet Format for Format_0, Format_1, Format_2, and Format_7

0-7	8-15	16-23		24-31	
data_length		tag	channel	tCode	sy
Data Length Number of bytes in the data field		**Tag Field** Set to 0	**Isochronous Channel Number** Programmed in the iso_channel field of the cam_sta_ctrl register	**Transaction Code** Set to the isochronous data block packet tCode	**Synchronization Value** Set to 0001h on the first isochronous data block of a frame, and set to zero on all other isochronous data blocks
header_CRC					
Video Data Payload Contains the digital video information					
data_CRC					

A.1 Isochronous Bandwidth Requirements: Format 0, Format 1, and Format 2

The amount of isochronous bandwidth required to transmit images from the camera is dependent on the format and frame rate. The following table describes the bandwidth requirements for each available format and frame rate. Each entry in the table indicates the required bandwidth in number of lines, pixels and 32-bits per isochronous period.

Note: Bandwidth requirements for Format 7 are negotiated with the camera at runtime.

Format_0

Mode	Video Format	240 FPS	120 FPS	60 FPS	30 FPS	15 FPS	7.5 FPS	3.75 FPS	1.875 FPS
0	160x120 YUV (4:4:4) 24bit/pixel	4H 640p 480q	2H 320p 240q	1H 160p 120q	1/2H 80p 60q	1/4H 40p 30q	1/8H 20p 15q		
1	320x240 YUV (4:2:2) 16bit/pixel	8)8H 2560p 1280q	4)4H 1280p 640q	2H 640p 320q	1H 320p 160q	1/2H 160p 80q	1/4H 80p 40q	1/8H 40p 20q	1/16H 20p 10q

Format_0

Mode	Video Format	240 FPS	120 FPS	60 FPS	30 FPS	15 FPS	7.5 FPS	3.75 FPS	1.875 FPS
2	640x480 YUV (4:1:1) 12bit/pixel	16)16H 10240p 3840q	8)8H 5120p 1920q	4)4H 2560p 960q	2)2H 1280p 480q	1H 640p 240q	1/2H 320p 120q	1/4H 160p 60q	1/8H 80p 30q
3	640x480 YUV (4:2:2) 16bit/pixel	32)16H 10240p 5120q	16)8H 5120p 2560q	8)4H 2560p 1280q	4)2H 1280p 640q	2)1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q	1/8H 80p 40q
4	640x480 RGB 24bit/pixel	32)16H 10240p 7680q	16)8H 5120p 3840q	8)4H 2560p 1920q	4)2H 1280p 960q	2)1H 640p 480q	1/2H 320p 240q	1/4H 160p 120q	1/8H 80p 60q
5	640x480 Y (Mono) 8bit/pixel	16)16H 10240p 2560q	8)8H 5120p 1280q	4)4H 2560p 640q	2)2H 1280p 320	1H 640p 160q	1/2H 320p 80q	1/4H 160p 40q	1/8H 80p 20q
6	640x480 Y (Mono) 16bit/pixel	32)16H 10240p 5120q	16)8H 5120p 2560q	8)4H 2560p 1280q	4)2H 1280p 640q	2)1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q	1/8H 80p 40q
7	Reserved								

Format_1

Mode	Video Format	240 FPS	120 FPS	60 FPS	30 FPS	15 FPS	7.5 FPS	3.75 FPS	1.875 FPS
0	800*600 YUV (4:2:2) 16bit/pixel	32)20H 16000p 8000q	16)10H 8000p 4000q	8)5H 4000p 2000q	4)5/2H 2000p 1000q	2)5/4H 1000p 500q	5/8H 500p 250q	5/16H 250p 125q	
1	800x600 RGB 24bit/pixel		32)10H 8000p 600q	16)5H 4000p 3000q	8)5/2H 2000p 1500q	4)5/4H 1000p 750q	2)5/8H 500p 375q		
2	800x600 Y (Mono) 8bit/pixel	16)20H 16000p 4000q	8)10H 8000p 2000q	4)5H 4000p 1000q	2)5/2H 2000p 500q	5/4H 1000p 250q	5/8H 500p 125q		
3	1024x768 YUV (4:2:2) 16bit/pixel		32)12H 12288p 6144q	16)6H 6144p 3072q	8)3H 3072p 1536q	4)3/2H 1536p 768q	2)3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q
4	1024x768 RGB 24bit/pixel			32)6H 6144p 4608q	16)3H 3072p 2304q	8)3/2H 1536p 1152q	4)3/4H 768p 576q	2)3/8H 384p 288q	3/16 192p 144q
5	1024x768 Y (Mono) 8bit/pixel	32)24H 24576p 6144q	16)12H 12288p 3072q	8)6H 6144p 1536q	4)3H 3072p 768q	2)3/2H 1536p 384q	3/4H 768p 192q	3/8H 384p 96q	3/16H 192p 48q
6	800x600 Y (Mono16) 16bit/pixel	32)20H 16000p 8000q	16)10H 8000p 4000q	8)5H) 4000p 2000q	4)5/2H 2000p 1000q	2)5/4H 1000p 500q	5/8H 500p 250q	5/16H 250p 125q	
7	1024x768 Y (Mono16) 16bit/pixel		32)12H 12288p 6144q	16)6H 6144p 3072q	8)3H 3072p 1536q	4)3/2H 1536p 768q	2)3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q

Format_2

Mode	Video Format	120 FPS	60 FPS	30 FPS	15 FPS	7.5 FPS	3.75 FPS	1.875 FPS
0	1280x960 YUV(4:2:2) 16bit/pixel		32)8H 10240p 5120q	16)4H 5120p 2560q	8)2H 2560p 1280q	4)1H 1280p 640q	2)1/2H 640p 320q	1/4H 320p 160q
1	1280x960 RGB 24bit/pixel		32)8H 10240p 7680q	16)4H 5120p 3840q	8)2H 2560p 1920q	4)1H 1280p 960q	2)1/2H 640p 480q	1/4H 320p 240q
2	1280x960 Y (Mono) 8bit/pixel	32)16H 20480p 5120q	16)8H 10240p 2560q	8)4H 5120p 1280q	4)2H 2560p 640q	2)1H 1280p 320q	1/2H 640p 160q	1/4H 320p 80q
3	1600x1200 YUV(4:2:2) 16bit/pixel		32)10H 16000p 8000q	16)5H 8000p 4000q	8)5/2H 4000p 2000q	4)5/4H 2000p 1000q	2)5/8H 1000p 500q	5/16H 500p 250q
4	1600x1200 RGB 24bit/pixel			32)5H 8000p 6000q	16)5/2H 4000p 3000q	8)5/4H 2000p 1500q	4)5/8H 1000p 750q	2)5/16H 500p 375q
5	1600x1200 Y (Mono) 8bit/pixel	32)20H 32000p 8000q	16)10H 16000p 4000q	8)5H 8000p 2000q	4)5/2H 4000p 1000q	2)5/4H 2000p 500q	5/8H 1000p 250q	5/16H 500p 125q
6	1280x960 Y (Mono16) 16bit/pixel		32)8H 10240p 5120q	16)4H 5120p 2560q	8)2H 2560p 1280q	4)1H 1280p 640q	2)1/2H 640p 320q	1/4H 320p 160q
7	1600x1200 Y(Mono16) 16bit/pixel		32)10H 16000p 8000q	16)5H 8000p 4000qH	8)5/2H 4000p 2000q	4)5/4H 2000p 1000q	2)5/8H 1000p 500q	5/16H 500p 250q

[--H – Lines/Packet]

[--p – Pixels/Packet]

[--q – 32-bits/Packet

2) : required S200 data rate
4) : required S400 data rate
8) : required S800 data rate
16) : required S1600 data rate
32) : required S3200 data rate

Appendix B: Dragonfly-only Registers

The following registers are used by the Dragonfly camera only and are not available on other cameras, including the Dragonfly2.

- EXTENDED_SHUTTER 1028h
- SOFT_ASYNC_TRIGGER 102Ch
- BAYER_TILE_GAIN 1044h
- SHUTTER_DELAY 1108h
- FRAME_TIME 1240h
- FRAME_SYNC_OFFSET 1244h

B.1 EXTENDED_SHUTTER: 1028h

Allows the user to access a number of different extended shutter modes. Placing the camera into extended shutter mode removes the restriction that the shutter integration time must be less than the frame rate. The actual frame rate will be the maximum of the nominal frame rate and the shutter time. Turn FRAME_RATE register OFF to enable extended shutter.

The maximum shutter values for the various modes are as follows:

Frame Rate	Maximum Shutter Value
30 Hz	532 * 1/16000 seconds
32 Hz	500 * 1/1600 seconds
Extended Shutter	4000 * 1/16000 seconds
50 Hz	256 * 1/12800 seconds
24 Hz	666 * 1/16000 seconds

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-12]	Reserved
Shutter_Mode	[13-15]	0: 30 Hz (Default) 1: 32 Hz 2: Extended Shutter 3: 50 Hz 4: 24 Hz
	[16-31]	Reserved

Related Resources

Type	Description
Software	*ExtendedShutterEx* example program (PGR FlyCapture SDK)

B.2 SOFT_ASYNC_TRIGGER 102Ch

Provides a software method for generating an asynchronous trigger event. When the camera is in Trigger_Mode_0, writing a zero to bit 31 of this register will generate an asynchronous trigger.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-29]	Reserved
Shutter_Mode	[30-31]	Write: 0: Generate Trigger Read: 0: Camera is not ready to be triggered; integration is complete but camera is transferring image data 1: Camera is ready to be triggered 2: Camera is in the middle of integration

Related Knowledge Base Articles

Title	Article
Time between software asynchronous trigger and start of integration	Knowledge Base Article 10089

Related Resources

Type	Description
Software	*AsyncTriggerEx* example program (PGR FlyCapture SDK)

B.3 BAYER_TILE_GAIN 1044h

Allows the user to specify all four Bayer tile pixel gains. The ordering matches that of the BAYER_TILE_MAPPING register (offset 1040h) and the units match those of the WHITE_BALANCE register (offset 80Ch).

Any write to this register will set the On_Off bit of the WHITE_BALANCE register.

Format:

Field	Bit	Description
Bayer_Gain_A	[0-7]	Gain for pixel (0,0) in the Bayer tile
Bayer_Gain_B	[8-15]	Gain for pixel (0,1) in the Bayer tile
Bayer_Gain_C	[16-24]	Gain for pixel (1,0) in the Bayer tile
Bayer_Gain_D	[25-31]	Gain for pixel (1,1) in the Bayer tile

B.4 SHUTTER_DELAY 1108h

This register provides control over the time delay between an external trigger and the start ofintegration (shutter open).

Format:

Field	Bit	Description
	[0-15]	Reserved
Shutter_Delay	[16-31]	Delay before the start of integration, in ticks of a 49.152 MHz clock. To extend the duration of this delay, use the Strobe_Multiplier defined in the GPIO_XTRA register.

B.5 FRAME_TIME 1240h

This register provides control over frame rate relative to the CURRENT_FRAME_RATE value.

For example, when CURRENT_FRAME_RATE = 4 (i.e. 30Hz on a lo-res Dragonfly) the camera sends 240 iso packets per image. To achieve 30Hz operation the camera waits for about 26-27 iso periods before sending the next image.

The FRAME_TIME register allows the desired frame rate to be specified, which could be considerably less than the nominal rate specified by CURRENT_FRAME_RATE. For example, with a CURRENT_FRAME_RATE of 30fps, 25fps is now possible.

The formula to determine the Value is:

FRAME_TIME = 800 * (Current_Frame_Rate / Desired_Frame_Rate)

Example:

To achieve 25fps while the current frame rate is 30fps:

FRAME_TIME = 800 * (30fps / 25fps)
= 960 = 3C0h

Enter 3C0h in the Value field (last 16 bits) of 1240h to achieve 25fps.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Always ON To turn this feature OFF, write a 0 to this bit and bits 20-31.
	[7-19]	Reserved
Value	[20-31]	Value.

B.6 FRAME_SYNC_OFFSET 1244h

Multiple cameras of the same type on the same IEEE-1394 bus are automatically synchronized to each other at the hardware level. This register allows the user to offset the synchronization of one camera relative to another camera by a defined amount of time. For example, it would be possible for camera "B" to always grab images 1ms after camera "A" grabs images; the two cameras are therefore synchronized, but the grabbing of "B" is delayed by 1 ms.

This register has the same format as the FRAME_TIME register and uses the same units. The offset must be some number between 0 and 1/- where - is the current frame rate. If the FRAME_TIME Value does not divide evenly into 128 seconds and the offset register is not written for all applicable cameras within the same 128s ISO period, setting a FRAME_SYNC_OFFSET Value will not work properly.

The formula to determine the FRAME_SYNC_OFFSET Value is:

$$\text{FRAME\_SYNC\_OFFSET} = \frac{\text{Desired\_Offset\_Time}}{(1 / \text{Current\_Frame\_Rate}) / \text{FRAME\_TIME\_Value}}$$

Example:

To determine the Value required to offset the synchronization of a camera running at 30Hz by 1 ms, read the FRAME_TIME register 1240h Value field. Assuming the Value is 320h:

$$\text{FRAME\_SYNC\_OFFSET} = \frac{0.001\text{s}}{(1 / 30\text{fps}) / 320\text{h}}$$

$$= 0.001\text{s} / 0.0000416\text{s/unit}$$

$$= 24 = 18\text{h}$$

Enter 18h in the Value field of 1244h to offset that camera's synchronization by 1 ms.

Contacting Us

For any questions, concerns or comments please contact us via the following methods:

Email	General questions Technical support (existing customers only)
Knowledge Base	Find answers to commonly asked questions in our Knowledge Base
Downloads	Download the latest documents and software
Contact Information	Contact Us on our website

Revision History

Revision	Date	Notes
2.1	August 2, 1007	Added Revision History Renamed to Point Grey Digital Camera Register Reference Added: 12E0h, 12E4, 1800h - 1484h, 1A14h, 1A60h, 1AC8 Added: Trigger Mode 15 Removed Feature Availability tables where register implements Presence_Inq field, or where a separate feature inquiry register is present (e.g. BRIGHTNESS_INQUIRY)
2.2	November 15, 2007	Updated FRAME_INFO for the FFMV
2.3	October 10, 2008	Added 12E8h Updated 12F8h, 1880h, 1884h
2.4	January 9, 2009	Updated 1F24h, 12F8h
2.5	March 2, 2009	Updated 1F24h
2.6	June 1, 2009	Updated GPIO Mode 4, 12F8h, 1100h, 1048h
2.7	August 28, 2009	Updated GPIO_CTRL_PIN, 12F8h, Trigger mode 14, Absolute Value Registers
2.8	November 24, 2010	Updated 62Ch, 12F8h
3.0	July 18, 2012	Reorganization of document Minor edits for clarification and format
3.1	February 6, 2013	Added registers for Iris, P-Iris, JPEG CTRL, JPEG Buffer (Ladybug only), GPIO Control, Output Voltage (Blackfly only)
3.2	June 4, 2015	Added 11F0h, 12E8h and 1048h back in as support for IIDC 1.31 Added new registers 5420h and 5424h for removing parameter limits. Minor edits and bug fixes for clarification and cross referencing.
4.0	January 2017	New template Bug fixes